AlGaN/GaN HEMTs grown by Molecular Beam Epitaxy on sapphire, SiC, and HVPE GaN templates

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ABSTRACT

Molecular Beam Epitaxy of GaN and related alloys is becoming a rival to the more established Metalorganic Vapor Phase Epitaxy. Excellent control of impurity, interface abruptness, and in-situ monitoring of the growth are driving the increase in quality of MBE epilayers. We have developed nucleation schemes with plasma-assisted MBE on three types of substrates, consisting of sapphire, semi-insulating (SI-) SiC, and HVPE SI-GaN templates on sapphire. While sapphire and SI-SiC are established substrates for the growth of AlGaN/GaN HEMT epilayers, HVPE GaN templates may provide a path to low-cost large-diameter substrates for electronic devices.
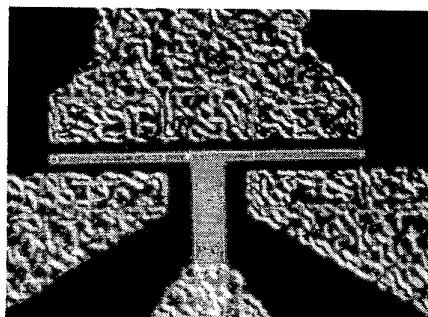
Figure 1: Micrograph of finished HEMT device, 2 fingers of 2μm x 25μm gates each

We compare device results of HEMTs fabricated on these substrates. As a metric for device performance, the saturated RF power output in class A operation is measured at 2 GHz. We achieved a saturated power density of 2.2 W/mm from HEMTs on sapphire, 1.1 W/mm from HEMTs on HVPE GaN templates on sapphire, and 6.3 W/mm from HEMTs on semi-insulating 6H-SiC substrates. The difference in output power can be attributed to self-heating due to insufficient thermal conductivity of the sapphire substrate, and to trapping in the compensation-doped HVPE template.

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INTRODUCTION

AlGaN/GaN HEMT devices have delivered extremely high RF output power densities at microwave frequency. Up to 11 W/mm have been demonstrated on MOCVD-grown AlGaN/GaN layers [1, 2], and up to 8 W/mm with layers grown by plasma-assisted MBE [3]. In the recent past, growth of AlGaN/GaN layers by MBE has received increased attention with the demonstration of high quality epilayer films. MBE growth offers certain advantages over MOCVD, such as very low background impurities, in-situ growth monitoring via RHEED, and the ability to produce atomically sharp interfaces. Epitaxy of GaN films is currently done mostly on foreign substrates, notably sapphire and SiC. The substantial lattice mismatch needs to be taken up in a dislocated buffer layer. The quality of the 2DEG, as measured by the Hall low field mobility, is largely dependent on the growth conditions at nucleation on the substrate, and during growth of the buffer layer.

We have developed nucleation layer schemes on both sapphire and SiC, involving a thin AlN layer deposited at the beginning of the growth. In both cases, the nucleation and subsequent growth of GaN result in films with Ga-face polarity, suitable for high-mobility AlGaN/GaN 2DEGs.
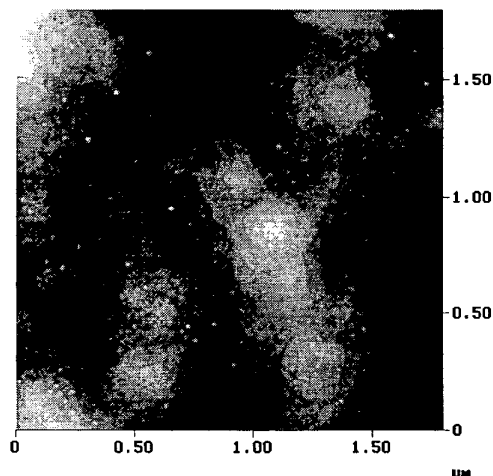

Figure 2: AFM image of MBE GaN/AlGaN heterostructure grown directly on sapphire
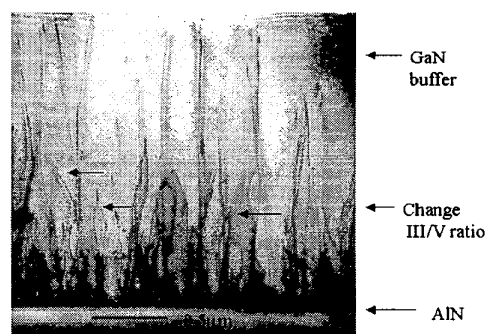

Figure 3: cross-sectional TEM of two-step GaN buffer on sapphire

The 2DEG properties can be further enhanced through buffer layer engineering. We developed a two-step growth process to reduce the number of extended defects present at the AlGaN/GaN interface, while keeping the surface smooth. A Ga/N ratio close to unity is chosen in the first half of the buffer growth. The slightly roughened surface leads to enhanced defect interaction due to the spatial proximity of neighboring defects. During the second half of the buffer growth, a Ga/N ratio greater than one is adjusted to smooth out the growth front (Figure 3). Only minimal defect interaction occurs in this regime, but the AlGaN/GaN interface is smooth (Figure 2), which minimizes interface roughness scattering.

GROWTH ON HVPE GaN TEMPLATES

Thick GaN templates grown by HVPE on sapphire substrates are used as a quasi-homoepitaxial substrate for the GaN MBE growth [4]. The threading dislocation at the surface of these templates is reduced to the 10^8 cm^{-2} range. We grow the MBE layer stack directly on top of the HVPE template without additional nucleation layers as in the case of growth on sapphire and SiC. As grown HVPE GaN is residually n-type due to Si and O impurities in the range of 10^{16} cm^{-3}.
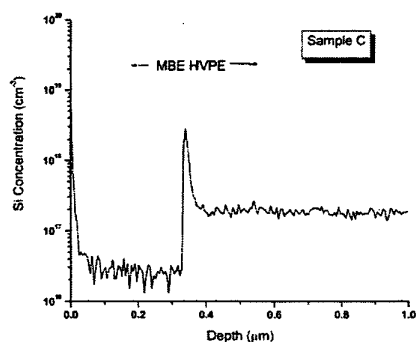

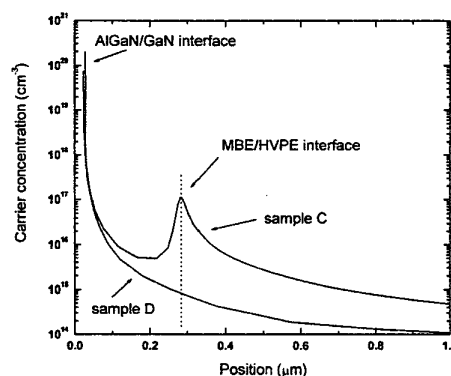Figure 4: SIMS profile of MBE GaN on HVPE GaN template

Figure 5: CV profile before (C) and after (D) correction of the compensation doping

To obtain semi-insulating layers, Zn is used as a compensating deep acceptor. A concentration of 10^{17} cm^{-3} Zn yields semi-insulating HVPE GaN layers. SIMS (Figure 4) and CV (Figure 5) profiling shows the absence of net dopants and charge at the HVPE/MBE interface. However, the buried HVPE nucleation layer is degenerately n-type. Thermal considerations are paramount for high-power microwave devices. Sapphire with its thermal conductivity of only 0.30 W/cmK limits the device output power severely.
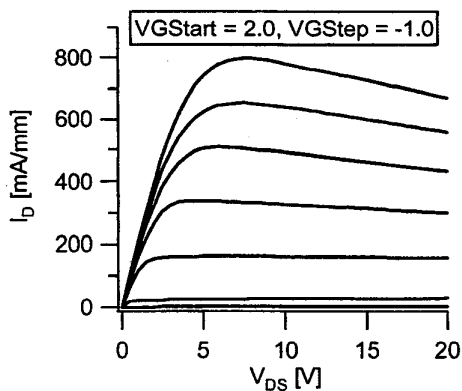

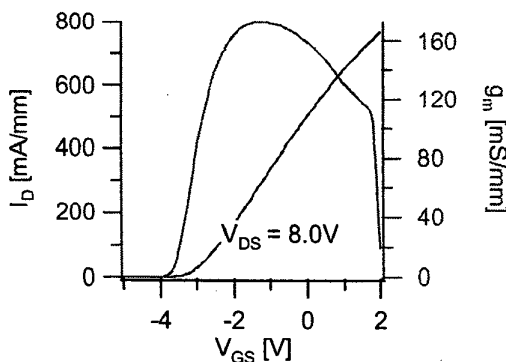
Figure 6: IV curve of HEMT on HVPE GaN

Figure 7: transfer characteristics of HEMT on HVPE GaN

A thick GaN layer helps spreading the heat conically under the active area of the power device, effectively decreasing the thermal impedance of the sapphire/GaN combination. Further enhancement may be reached with flip-chip package designs.

We were able to produce HEMT devices on these layers that show good pinch-off behavior, proving the absence of a parasitic channel in the HVPE template (Figure 6). Due to the low defect concentration in MBE layers grown on HVPE templates, we were able to measure record low-temperature mobilities for low-density 2DEGs up to 75,000 cm^2/Vs at 4K.
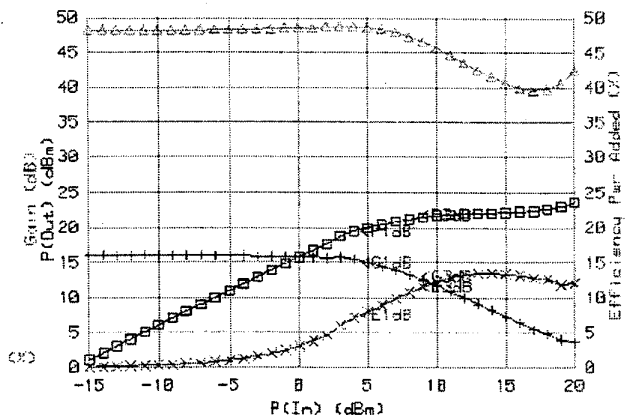

Figure 8: load-pull data of 200 μm wide HEMT on HVPE GaN

GROWTH DIRECTLY ON SAPPHIRE

Sapphire is still widely used as a substrate for GaN growth due to its low cost as compared to SiC, allowing for cost-effective development of device processing steps such as ohmic contact metallization. Using a thin AlN nucleation layer, we reproducibly yielded Ga-face AlGaN/GaN heterostructures [5] with mobilities higher than 1,200 cm^2/Vs at a carrier concentration of approximately 10^{13} cm^{-2}.
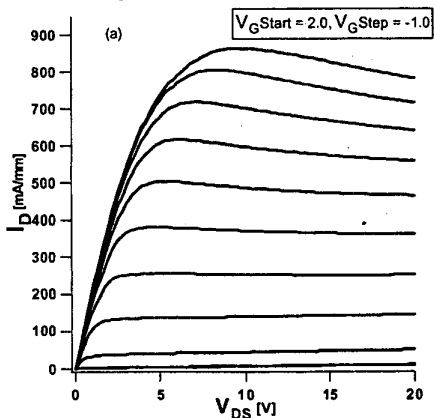

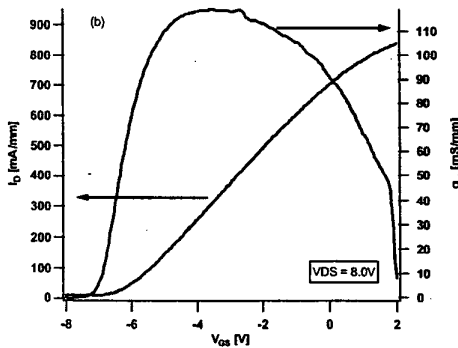Figure 9: IV curve of 100 μm wide HEMT on sapphire

Figure 10: transfer characteristics of 100 μm wide HEMT on sapphire

We fabricated HEMTs from these layers, DC data are shown in Figure 9 and Figure 10. The RF output power is limited by the thermal properties of the substrate. We obtained 2.2 W/mm at 2 GHz from a 100μm wide HEMT on sapphire (Figure 11) in class A device operation.
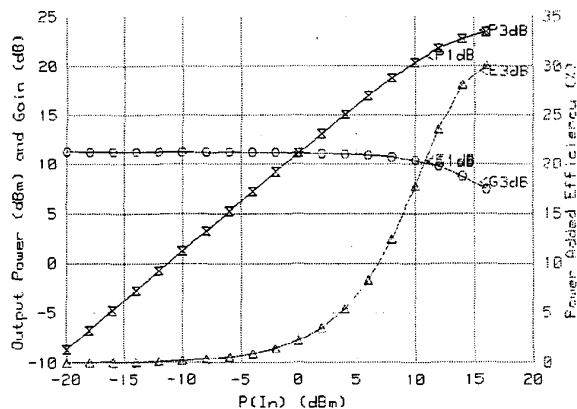

Figure 11: class A load-pull data of 100 μm wide HEMT on sapphire, $V_{DS} = 20V$, $I_{DS} = 266$ mA/mm

GROWTH ON SEMI-INSULATING 6H-SIC

SiC currently provides the best compromise in thermal management and lattice mismatch for epitaxial growth of GaN. We used semi-insulating 6H-SiC substrates from Sterling Semiconductor for our AlGaN/GaN HEMTs on SiC. Prior to MBE growth, the substrates receive an additional chemical mechanical polish.

Figure 12: IV curve of 25 μm wide HEMT on 6H-SiC
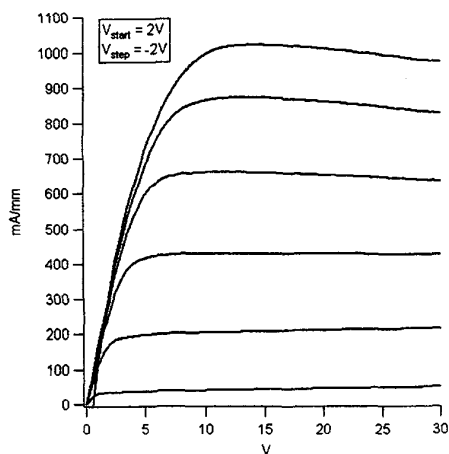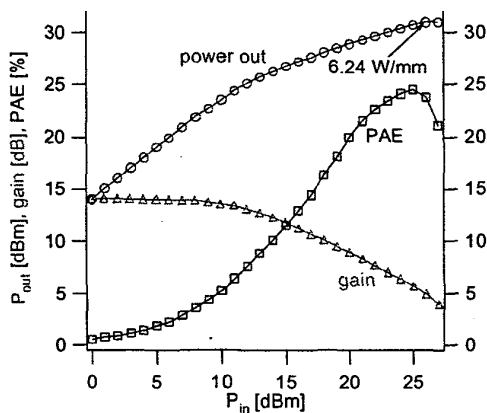

Figure 13: class A load pull data, 200 μm wide HEMT on 6H-SiC; VDS = 40V

A thin AlN film serves as a nucleation layer. Our standard AlGaN/GaN layer structure consists of approximately 2 μm of GaN, followed by a 25 nm thick $Al_{0.30}Ga_{0.70}N$ barrier, and a 5 nm thick undoped GaN cap. Part of the barrier is doped with silicon ($8\cdot10^{17}$ cm^{-3}) to reduce the

resistance of the ohmic contacts. At room temperature, we measure Hall mobilities higher than 1,300 cm^2/Vs and a sheet carrier concentration of $1.2 \cdot 10^{13}$ cm^{-2}, resulting in a sheet resistance approximately 350 $\Omega/\square$. We were able to reproducibly process HEMTs from these layers, with a saturated drain current of more than 1 A/mm. Most devices yielded a saturated output power of around 4.5 W/mm at 2 GHz. The best device showed a saturated output power of 6.2 W/mm with an associated gain of 5 dB. The power added efficiency was measured to 24%. All values were obtained from unpassivated devices in class A operating condition [6].
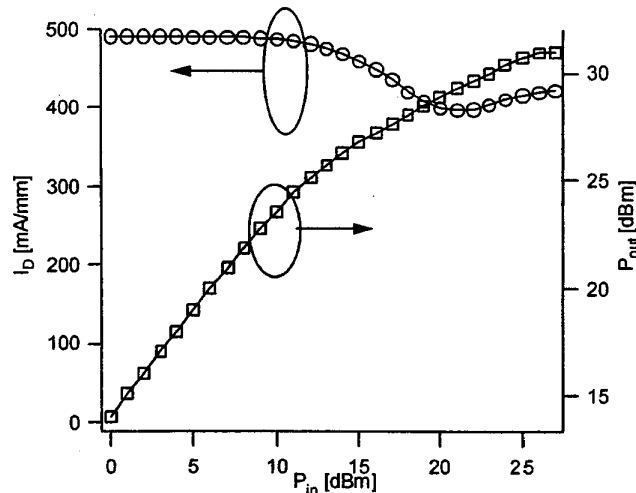

Figure 14: drain current dispersion of same device as shown in Figure 13

It is noteworthy that the drain current dispersion in these devices is very low, given the absence of a passivating layer. From Figure 14, a decrease of the DC drain current of only 17% from the small-signal regime towards saturation was recorded. At first, the drain current drops, until the drive signal voltage is large enough to bias the gate-source Schottky diode in forward direction, leading to rectification of the input signal and a positive shift of the internal gate bias, which increases the drain current.

HEMT DEVICE FABRICATION AND MEASUREMENT

HEMT devices are fabricated with optical lithography (Figure 1). The short turn-around time of our robust device process enables quick feedback to the epilayer growth. The devices are mesa-isolated in an ICP Chlorine etch step. Ohmic contacts are deposited by e-beam and thermal (Al) evaporation. We use Ti/Al/Ni/Au or Ti/Al/Ti/Au for our ohmic contact metallization. Transfer resistances as low as 0.3 Ω-mm have been realized, routinely we obtain 0.5 Ω-mm after rapid thermal annealing in nitrogen at 850°C. Finally, Schottky gates are deposited by e-beam evaporation of Ni followed by a thick Au layer. Presently, all our devices are *unpassivated* when measured.

The DC characteristics of the HEMTs are measured with an HP4145B semiconductor parameter analyzer. We measure saturated drain current densities of more than 1 A/mm on SiC and on HVPE GaN templates. On sapphire, we achieved a maximum drain current of 880 mA/mm. The gate leakage current is typically around 150 μA/mm in pinch-off at 20 V_{DS}. We obtained a

maximum transconductance of 180 mS/mm; in addition, the transconductance is relatively flat across a wide rage of gate voltages. Pinch-off occurs between −4 and −10 V_{GS}, depending on sheet charge and barrier structure. The devices break down at 95 V_{DS} (three-terminal breakdown). The RF power output is measured with an ATN LP1 automated load-pull measurement setup at 2 GHz. Small-signal S-parameters are recorded with an HP8510C network analyzer and an HP8516A test set in the passband of the tuners between 2 and 8 GHz. We extrapolated f_t/f_{max} of 6 and 16 GHz, respectively, for our devices with a gate length between 1 and 2 μm. We tested devices on all three substrates on various wafers. The highest saturated power densities we found at 2 GHz were 2.2 W/mm on sapphire, 1.1 W/mm on HVPE templates, and 6.2 W/mm on SiC for a device periphery of 200 μm, with a drain voltage between 35 and 45 V.

DISCUSSION

The power density on SiC is limited in part by the large drain-source separation of 6 μm in our simple test mask, limiting the power-added efficiency as well. On sapphire, the power density is limited by the thermal impedance of the substrate, as evidenced by the negative output conductance visible in the IV curve. We expected the output power of devices on HVPE GaN templates between sapphire and SiC; however, we recorded only 1.1 W/mm. The unionized excess Zn acceptors in the HVPE GaN may act as trapping centers, which can be charged and act as a backgate on the 2DEG. Drain dispersion defined as the variation of the DC drain current with RF input power at constant gate and drain bias voltage is measured for all three substrates. On SI-SiC substrates, we observed as little as 7% drop in drain current with input power. On HVPE GaN templates, the drain current drops by 20%, indicating trapping in the substrate. Additionally, the gain compresses prematurely. The 1dB compression point is reached at 19 dBm output power and 4 dBm input power for a device with 200 μm periphery. The maximum power-added efficiency is only 14% on HVPE templates in class A operation, compared to 25% on SI-SiC.

CONCLUSION

We have grown high-quality AlGaN/GaN HEMT device layers by plasma-assisted MBE on various substrates. The highest saturated output power of 6.2 W/mm was measured from unpassivated HEMT devices on SI 6H-SiC at 2 GHz in class A operation. Record low-field mobilities up to 75,000 cm^2/Vs were measured from AlGaN/GaN MBE films grown on GaN templates prepared by Hydride Vapor Phase Epitaxy.

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