Impact of Heterostructure Design on Transport Properties in the Second Landau Level of *In Situ* Back-Gated Two-Dimensional Electron Gases

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We report on transport in the second Landau level in *in situ* back-gated two-dimensional electron gases in GaAs/$Al_xGa_{1-x}As$ quantum wells. Minimization of gate leakage is the primary heterostructure design consideration. Leakage currents resulting in dissipation as small as ~10 pW can cause noticeable heating of the electrons at 10 mK, limiting the formation of novel correlated states. We show that when the heterostructure design is properly optimized, gate voltages as large as 4 V can be applied with negligible gate leakage, allowing the density to be tuned over a large range from depletion to over 4×10^{11} cm^{-2}. As a result, the strength of the $\nu = 5/2$ state can be continuously tuned from onset at $n \sim 1.2 \times 10^{11}$ cm^{-2} to a maximum $\Delta_{5/2} = 625$ mK at $n = 3.35 \times 10^{11}$ cm^{-2}. An unusual evolution of the reentrant-integer quantum Hall states as a function of density is also reported. These devices can be expected to be useful in experiments aimed at proving the existence of non-Abelian phases useful for topological quantum computation.

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I. INTRODUCTION

Since the discovery of the fractional quantum Hall effect (FQHE) at $\nu = 5/2$ [1], this state has drawn intense scrutiny. Much of the motivation for the study of the $\nu = 5/2$ state comes from the fact that numerical work [2–5] shows strong overlaps with the Pfaffian wave function [6] and its particle-hole conjugate state, the so-called anti-Pfaffian state [7,8], both of which are non-Abelian and could find uses in topologically protected quantum computation [9–11]. There have also, however, been theoretically proposed wave functions for the $\nu = 5/2$ state that exhibit Abelian statistics (see Refs. [12,13] for a summary of candidate states). To date, the experimental tests to determine the nature of the ground state at $\nu = 5/2$ fail to agree on the identity of the wave function. Experiments probing the temperature dependence of tunneling between the edge states at $\nu = 5/2$ have been proposed [14] and conducted [15,16] as a way to measure the quasiparticle effective charge e^* and Luttinger-liquid interaction parameter g in order to discriminate between proposed wave functions. These experiments, however, were inconclusive as tunneling experiments performed on the same Hall bar mesa but with different electrostatic confinement potentials gave results consistent with the non-Abelian anti-Pfaffian and $U(1) \times SU_2(2)$ states [15] and the Abelian 331 state [16]. Later experiments by a different group [17] are most consistent with the 331 state, but recent measurements of the spin polarization at $\nu = 5/2$ using NMR techniques [18,19] indicate a fully spin-polarized electron gas which is inconsistent with the unpolarized 331 state [20]. Interferometry experiments showing an alternating Aharanov-Bohm period [21,22] are also consistent with a non-Abelian state at $\nu = 5/2$ and thus appear to rule out the 331 state. As it is unclear how possible edge reconstruction [23] due to shallow confining potentials might influence the interpretation of the tunneling experiments, it is possible that the different confinement parameters in the previously studied devices could be responsible for this apparent discrepancy.

Given the complications associated with these experiments, it would therefore be desirable to examine transport in nanostructures in the quantum Hall regime in samples in which the electron density and confining potential could be tuned simultaneously in a single structure. A variable density would also allow for direct comparisons between experimental results in the second Landau level (LL) and the more well-understood lowest LL in a single device without the need for extremely large magnetic fields. In addition, the original proposal [24] for an edge-state interferometer designed to directly measure the quantum statistics of the quasiparticles at $\nu = 5/2$ calls for a device with a global back gate to allow magnetic field sweeps at a constant filling fraction. As such, there is strong motivation for back-gated devices exhibiting strong FQHE in the second LL concomitant with a large range of density tunability.

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II. DEVICE GROWTH AND FABRICATION

In order to undertake such experiments, however, it is necessary to have a thorough understanding of how heterostructure design and device-fabrication parameters affect device yields and the quality of transport in the second LL. Towards this aim, we grow and process a series of high-quality, *in situ* back-gated two-dimensional electron gases (2DEGs). The processing of similar devices of lower mobility has been reported [25–32] and a similar high-mobility device has been used to examine the energy gaps of FQHE states in the second LL [33]. However, none of these previous works reported a systematic study of the impact of heterostructure design and processing parameters on the visibility of the states in the second LL.

We study three wafers utilizing two heterostructure designs summarized in Fig. 1 to study the impact of the heterostructure on the gate leakage and the low-temperature transport. Both designs feature a 2DEG located approximately 200 nm from the surface in a 30-nm GaAs quantum well flanked by $Al_{0.24}Ga_{0.76}As$ barrier modulation doped from the top side only at a setback of ~70 nm. The dopants are incorporated into a so-called doping-well scheme (also known as a short-period superlattice) [34–37] which has been found empirically to maximize the FQHE energy gaps in the second LL. The *in situ* gate consists of an n^+ GaAs layer situated 850 nm below the bottom interface of the quantum well. The key difference between the two designs is that in design 1 an $Al_{0.24}Ga_{0.76}As$ barrier of thickness $t_b = 200$ nm separates the quantum well from a GaAs/AlAs (2/2 nm) superlattice, while in design 2 t_b is decreased to 20 nm while keeping the overall gate setback fixed at 850 nm. Wafers *A* and *B* utilize design 1 while wafer *C* utilizes design 2.

Device fabrication begins by etching via holes to the gate layer using an etchant consisting of 50:5:1 water: phosphoric:peroxide followed by a second, ~160-nm-deep etch to define 1 mm van der Pauw square mesas. Ohmic contacts consist of a 8/80/160/36 nm stack of Ni/Ge/Au/Ni and are annealed for 1 min in forming gas at a variety of temperatures. Following the annealing, large

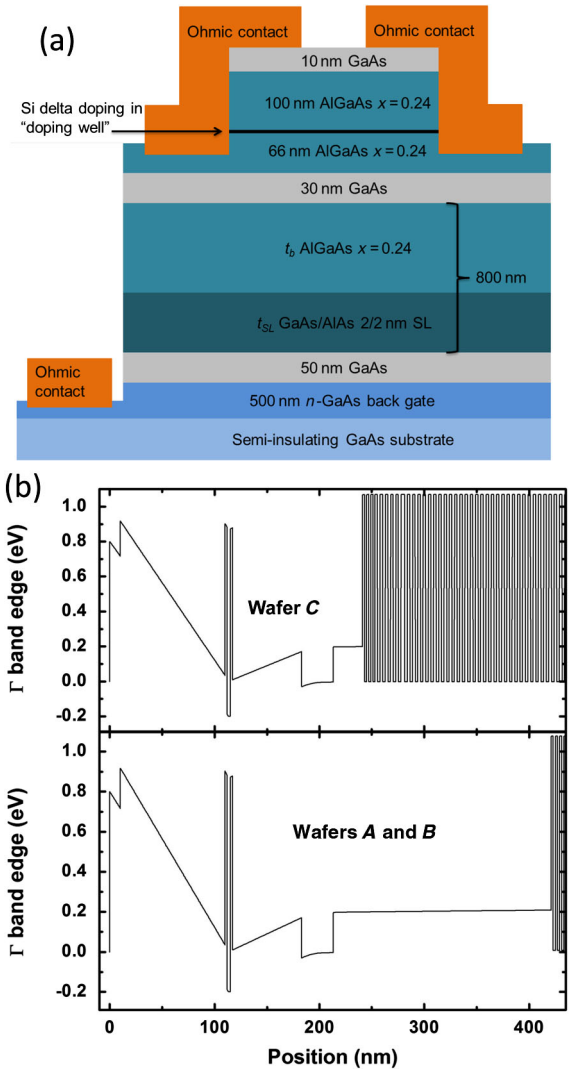

FIG. 1 (color online). Heterostructure and device design. (a) Cross section of device showing heterostructure layer sequence and lithographic design. Dimensions are not to scale. Two separate etch steps define "via" holes to the back gate and the van der Pauw mesa. Ohmic contacts to the 2DEG and the gate are deposited in a single evaporation. TiAu pads (not shown for clarity) are deposited after the Ohmic contacts to facilitate wire bonding. (b) Self-consistent Schrödinger-Poisson calculation of band structure showing the different position of the superlattice in each wafer.

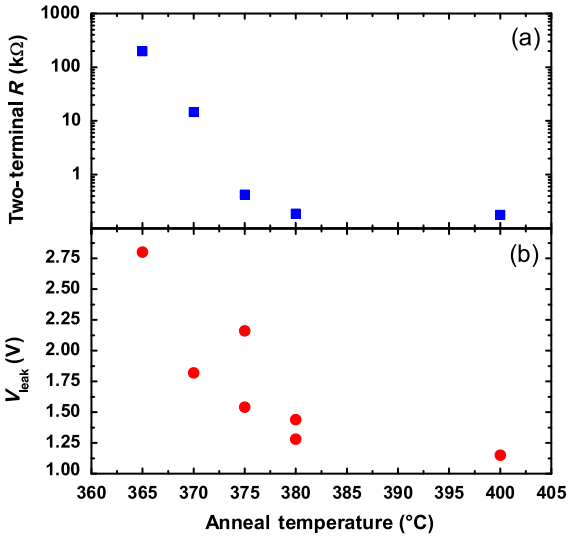

FIG. 2 (color online). Effect of Ohmic annealing temperature on device performance from wafer *A*. (a) Median two-terminal resistance to ground of individual contacts measured in the dark at $T = 4$ K and $V_g = 0$ as a function of annealing temperature. (b) V_{leak}, defined as the voltage at which the gate-leakage current reaches 1 nA, as a function of annealing temperature. Two data points each are shown at 375 and 380 °C as this is near the optimal annealing temperature.

TiAu pads off of the mesa are deposited in order to facilitate wire bonding.

Figure 2 shows the effect of annealing temperature on the quality of the contacts and the gate leakage measured in the dark at $T = 4$ K on devices fabricated from wafer B. The lead resistance of the measurement setup is $\sim 1\ \Omega$, so the two-terminal resistance values quoted here are reasonable proxies for the true contact resistance. At an annealing temperature of 360 °C, the contacts are electrically open at low temperature, and the contact morphology is extremely smooth, indicating that the metal does not melt or diffuse significantly during the anneal. Figure 2(b) displays the effect of the annealing on the gate leakage. To quantify the leakage from our devices, we define V_{leak} as the gate voltage V_g at which the gate-leakage current reaches 1 nA; thus high values of V_{leak} are expected for a high-quality gate-insulating layer. Both the two-terminal resistance and V_{leak} decrease monotonically as the annealing temperature is increased and the NiAuGe diffuses further into the semiconductor.

To further study the impact of mask design and processing parameters on the gate leakage and contact resistance, we fabricate a set of test structures (not shown) which give evidence that the gate leakage is primarily through the annealed contacts and not through the bulk of the mesa. In addition, the test structures give evidence that the leakage-current density through annealed metal in etched regions is larger than that through annealed metal in unetched regions. The increased electric field due to the decreased gate-contact separation in the etched regions is insufficient to account for this increase in leakage density. This observation appears to imply that the etching procedure enhances the subsequent diffusion of the contacts. With this in mind, we design our lithographic mask sets to minimize the total Ohmic area, particularly in the region off of the etched mesa. In our final design the total Ohmic area is $<1.5 \times 10^4\ \mu\mathrm{m}^2$ per device, and the total Ohmic overhang off each mesa is $\sim 6000\ \mu\mathrm{m}^2$. By minimizing the total time the etched sidewall of the mesa is exposed to air between the etch step and the metallization (typically ~3–4 h) and optimizing the geometry of the Ohmic contacts to include 45° scallops, we are able to produce devices with acceptably low contact resistances in the range of a few hundred Ohms while minimizing the gate leakage.

Next, we examine the impact of heterostructure design on device performance. Using our optimized fabrication recipe and mask set, we fabricate devices on both wafers B and C, using an annealing temperature of 375 °C. Figure 3 is a histogram of the leakage turn-on V_{leak} for devices from each wafer. The leakage in the majority of devices from wafer B (black bars) turns on around 2.2 V while the leakage in devices from wafer C (red bars) typically turns on around 3.8 V. Evidently, the proximity of the superlattice to the quantum well has a pronounced effect on the gate leakage.

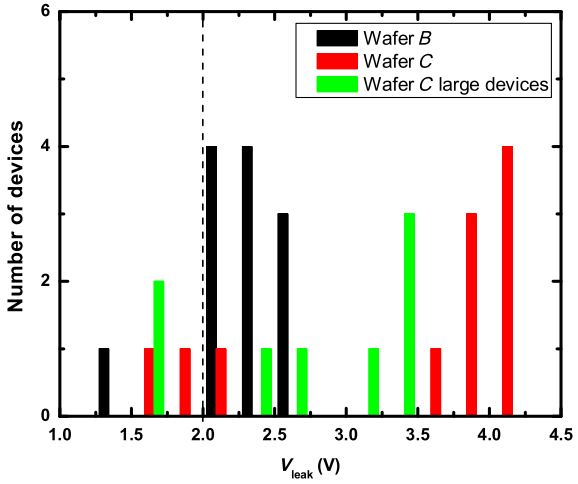

FIG. 3 (color online). Histogram of leakage turn-on voltage V_{leak} for devices fabricated with the optimized processing recipe and mask set. All the devices are annealed at 375 °C. The dashed line represents the voltage required to reach a 2DEG density of $\sim 3.2 \times 10^{11}\ \mathrm{cm}^{-2}$.

The dashed line in Fig. 3 represents the gate voltage required in our geometry to reach a 2DEG density of $\sim 3.2 \times 10^{11}\ \mathrm{cm}^{-2}$, roughly twice the zero-bias density and the approximate electron density of 2DEGs exhibiting state-of-the-art energy gaps in the second LL (see, for instance, Refs. [37–39]). As the devices from wafer C clearly could be biased well beyond the point necessary to study the FQHE of the second LL, we fabricate Hall bar devices with larger contacts on wafer C to check how much less stringent the device design and fabrication requirements are for this wafer to exhibit acceptable gate leakage. These devices are based on a design [40] known to both exhibit high-quality transport in the second LL and allow the incorporation of nanostructures. The total Ohmic area per device is $3.0 \times 10^5\ \mu\mathrm{m}^2$ with $4.6 \times 10^4\ \mu\mathrm{m}^2$ overhanging the edge of the mesa. Even though the Ohmic area in the etch field increases by a factor of ~8 and the total Ohmic area increases by a factor of ~20 from our optimized mask design, the leakage turn-on in most devices is still beyond 2.5 V, further highlighting the importance of proper heterostructure design.

We speculate that the large reduction in gate leakage in wafer C is due to two effects. First, the alternating layers of the superlattice act as a diffusion barrier [41,42] to the metal from the Ohmic contacts; thus, by moving the superlattice closer to the quantum well, less metal is able to diffuse towards the gate, thereby reducing the shorting of the Ohmics to the gate. In addition, Fowler-Nordheim tunneling [43–47] from the bulk of the 2DEG to the gate can be expected to be reduced by moving the tall AlAs barriers of the superlattice closer to the 2DEG.

While moving the superlattice closer to the quantum well has the benefit of dramatically increasing the maximum

achievable density, it also has the undesirable consequence of placing a significant amount of AlAs close to the quantum well. It is known that Al is an effective getter of vacuum impurities during MBE growth [35], and thus moving the superlattice closer to the 2DEG may degrade the quality of the FQHE states. Indeed, the average maximum electron mobility in devices from wafer B is $\sim 15 \times 10^6$ cm^2/V s while that from wafer C is $\sim 11 \times 10^6$ cm^2/V s. Wafers B and C are grown on the same day, so it appears likely that the decrease in mobility can be attributed to the change in heterostructure design. That being said, it has become clear in recent years that the zero-field mobility is not a good predictor of energy gaps in the second LL [33,37,38,48]. Consequently, it is necessary to examine the magnetotransport at low temperature to make any definitive statement on the potential negative impact of moving the superlattice closer to the 2DEG.

III. IMPACT OF HEAT SINKING AND HETEROSTRUCTURE DESIGN ON RIQHE STATES

Figure 4 illustrates the importance of minimizing the gate leakage and properly heat sinking the sample in order

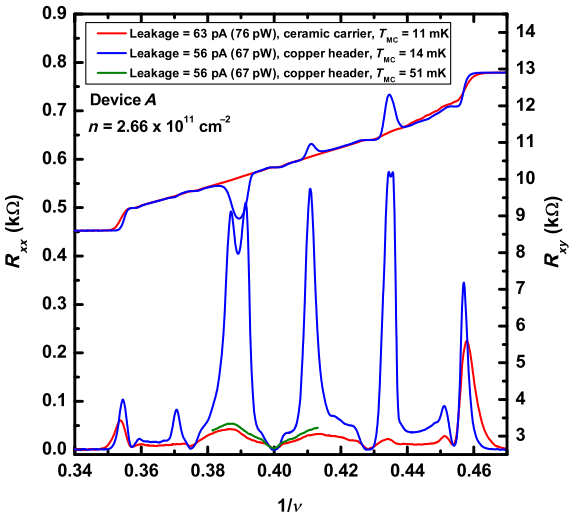

FIG. 4 (color online). Magnetotransport in the lower-spin branch of the second LL in device A after illumination with a red LED. During the first cooldown of the sample (red curves) the sample was mounted on a commercial ceramic chip carrier. At a gate-leakage current (power) of ~63 pA (76 pW) the electrons appear very warm as seen by the lack of RIQHE features, despite a low mixing chamber temperature T_{MC}. During the second cooldown of the sample (blue curves), the device was mounted on a homemade header with a copper strip screwed onto the end of the cold finger on the mixing chamber. The electrons were obviously much colder even for a slightly higher T_{MC}. The green curve shows the transport around $\nu = 5/2$ during the second cooldown for $T_{\mathrm{MC}} = 51$ mK. Comparing the green and black data, we conclude that the electron temperature was ~50 mK for $T_{\mathrm{MC}} = 11$ mK during the first cooldown.

to study the second LL at low temperatures ($T < 25$ mK). The data shown are taken from an early device from wafer A which was fabricated prior to the final optimization of our processing recipe. During the first cooldown of the device, the Joule heating of the electrons due to the gate-leakage current evidently caused the electron temperature to depart from the mixing chamber temperature T_{MC} for a gate-leakage current (power) ~4 pA (~3.5 pW) as evinced by weakening of the reentrant-integer quantum-Hall-effect (RIQHE) features (data not shown). By contrast, the excitation current of 2.1 nA contributed a negligible power dissipation of ~45 fW at $\nu = 5/2$. In order to facilitate wire bonding, we mounted the device on a commercial bondable ceramic chip carrier during the first cooldown. This meant, however, that the sample was only cooled through the 18-μm-thick Au bond wires. To improve the heat sinking, we rewired the same device on a homemade header. In this design the sample is mounted to a strip of Cu with Ag paint, and the Cu strip is screwed directly onto the Cu cold finger of the mixing chamber resulting in a continuous metal connection between the mixing chamber and sample. With this improved heat sinking, heating of the electrons is not evident until a gate-leakage current (power) ~56 pA (67 pW). Figure 4 illustrates the vast improvement in electron temperature achieved by improving the heat sinking of the sample. For a fixed density and approximately constant gate-leakage current, the data taken with the Cu strip header show strong RIQHE features while the data taken with the ceramic chip carrier show no RIQHE features. To quantify T_{electron} during the first cooldown, we show data (green curve in Fig. 4) taken at $T_{\mathrm{MC}} = 51$ mK during the second cooldown. The insulating peaks in R_{xx} in the vicinity of $\nu = 5/2$ at $T_{\mathrm{MC}} = 51$ mK during the second cooldown are comparable to those seen at $T_{\mathrm{MC}} = 11$ mK during the first cooldown. This allows us to estimate $T_{\mathrm{electron}} \sim 50$ mK for the black curves in Fig. 4.

After optimizing our fabrication recipe, we cooled one exemplary device each from wafers B (device B) and C (device C) to low temperature (<25 mK) to examine the transport as a function of density at low temperature. The RIQHE states in device C (from wafer C) show an interesting evolution with density as shown in Fig. 5. In order to quantitatively compare the states, we define the strength S of the RIQHE states as

$$S \equiv \frac{|R_{xy}^{c} - R_{xy}|}{|R_{xy}^{c} - R_{xy}^{i}|}, \tag{1}$$

where R_{xy}^{c} is the classical Hall resistance at the filling fraction of interest, R_{xy} is the actual Hall resistance at the peak position, and R_{xy}^{i} is the resistance of the nearest integer Hall plateau. Using this definition, a fully quantized RIQHE state has a strength of 1 while a completely absent state has a strength of 0. Figure 5 shows the evolution of the

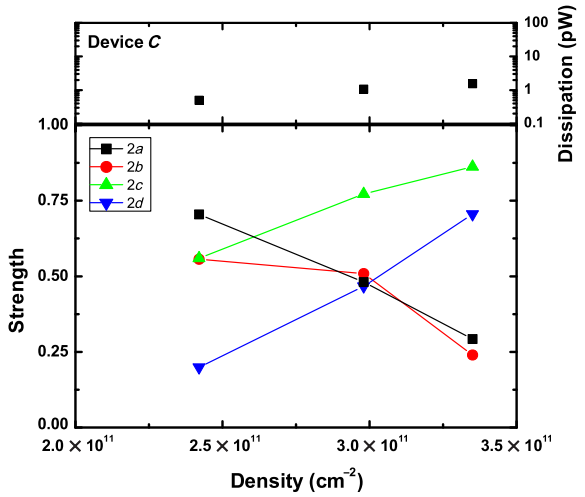

FIG. 5 (color online). Strength (as defined in the text) of the RIQHE in device C during the second cooldown as a function of density; the power dissipation from the gate-leakage current is shown in the top panel. States $2a$ and $2b$ weaken over the measured density range while states $2c$ and $2d$ strengthen over the same range. See Fig. 7 for labels of each RIQHE state.

RIQHE states in device C during its second cooldown. The states on the high-field side of $\nu = 5/2$, $2a$ and $2b$ ($\nu \sim 2.29$ and 2.42, respectively), are seen to weaken over the measured density range while states $2c$ and $2d$ ($\nu \sim 2.56$ and 2.70, respectively) continue to strengthen. Figure 6 shows a comparison of the evolution of state $2a$ in device C as a function of density for two different cooldowns. Even though the power dissipation from the gate leakage varies by ~1 order of magnitude between the two cooldowns (possibly due to slightly different illumination conditions), the data show the same trend. Comparisons between the

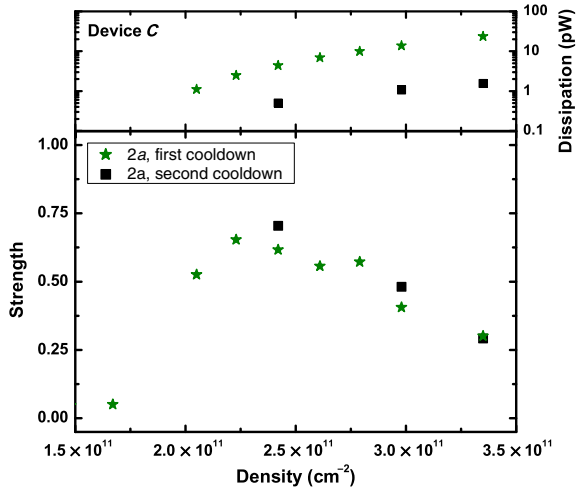

FIG. 6 (color online). Comparison of the strength of the $2a$ RIQHE state in device C from two different cooldowns. The strength of the state is comparable between the two cooldowns despite the large change in gate power dissipation.

TABLE I. Summary of gate power dissipation in each device around the threshold of observable heating in the RIQHE states. P_1 is defined as the power dissipation with the strongest measured RIQHE states and P_2 is defined as the power dissipation at which *all* the RIQHE states are first observed to weaken with increasing density.

Device	P_1 (pW)	P_2 (pW)
A, copper header	1.5	67
B, copper header	6.4	114
C, copper header	1.6	38

other three states for the two cooldowns show similar agreement. This appears to indicate that the observed evolution in strength is driven primarily by the 2DEG density and not by heating from the gate leakage. At present, the origin of this behavior is not understood. Regardless of the mechanism that causes states $2a$ and $2b$ to weaken with increasing density, this behavior is qualitatively different from that seen in states $2c$ and $2d$ and may point to a difference in the underlying localization mechanisms. In contrast, the strength of all the RIQHE states in device B (from wafer B) with the larger superlattice setback (data not shown) is seen to increase with density up to a density (power dissipation) of 2.67×10^{11} cm^{-2} (6.4 pW) after which all the RIQHE states weakened. While we cannot identify the mechanisms that alter localization, it appears that the different proximity of the superlattice to the 2DEG in wafers B and C has a significant impact.

Finally, to estimate the maximum acceptable power dissipation, we summarize the measured data points on either side of the heating threshold at which *all* the RIQHE states start to weaken with increasing density in Table I. Given that the maximum strength in device B is observed for a power dissipation of 6.4 pW and the RIQHE states in device C have begun to weaken by 38 pW, we set ~10 pW as the upper bound on acceptable power dissipation from the gate in our devices given the setup of our cryostat. This extremely low power level serves to highlight the necessity of minimizing the gate leakage in order to study the second LL.

IV. IMPACT OF HETEROSTRUCTURE DESIGN ON THE FQHE STATES

We now turn to the central result of our work. Figure 7 shows low-temperature transport ($T_{MC} \sim 10$ mK) at two different densities for device C after illumination with a red LED. The device shows excellent transport with all four RIQHE states present and well-developed FQHE states at $\nu = 14/5$, $8/3$, $5/2$, and $7/3$. In addition, nascent states at $\nu = 12/5$ and $\nu = 2 + 6/13$ begin to develop at high density. The observation of these states, despite their extreme fragility [49–51], in a back-gated sample points to the high quality of the 2DEG. The presence of the state at

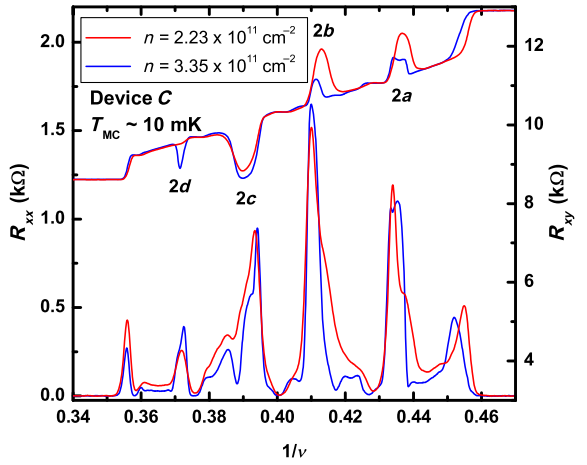

FIG. 7 (color online). Magnetotransport in device C after illumination with a red LED. The reentrant states are labeled following the convention in Ref. [52]. Red data show the transport for the maximum strength in RIQHE states $2a$ and $2b$, while the blue data show transport at the highest density before the second subband became occupied.

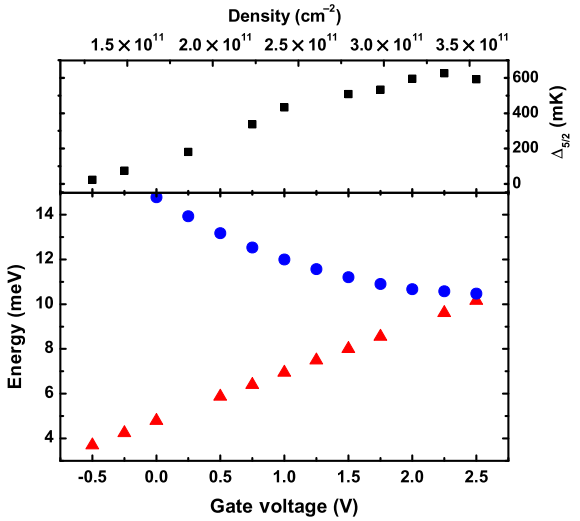

FIG. 9 (color online). Cyclotron energy $\hbar\omega_c$ (red triangles) and spacing between E_F and the second subband (blue circles) overlaid with $\Delta_{5/2}$ for wafer C. $\Delta_{5/2}$ drops suddenly at high density when the ground state is pushed into the lowest LL of the antisymmetric subband.

$\nu = 12/5$ is particularly interesting as this state has been proposed as a host of Fibonacci anyons which could be used for universal topological quantum computation [11].

We examine the strength of the FQHE in each device quantitatively by measuring the gap at $\nu = 5/2$ ($\Delta_{5/2}$). Figure 8 displays the gap at $\nu = 5/2$ as a function of density for devices B and C. It is clear that, within the experimental resolution, the gaps are nearly identical for both devices at low density ($n < 2.5 \times 10^{11}$ cm^{-2}). Evidently, neither the day-to-day variation in the MBE growth conditions nor the uncontrolled sample degradation from device fabrication nor the proximity of the superlattice to the 2DEG significantly affect the gap at $\nu = 5/2$. Device

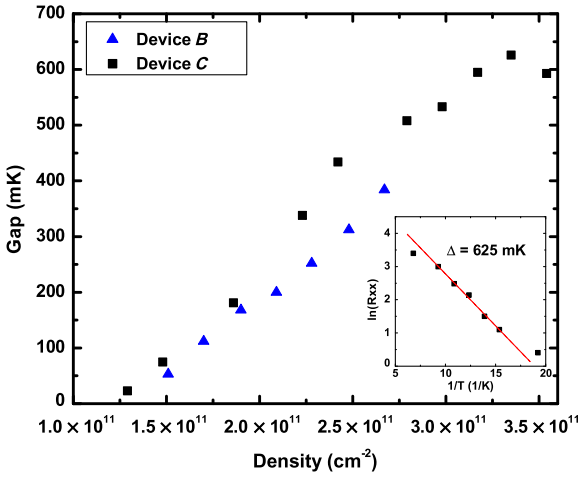

FIG. 8 (color online). Gap at $\nu = 5/2$ as a function of density for devices B and C. The inset shows the Arrhenius plot for device C at a density of 3.35×10^{11} cm^{-2} where the gap is measured to be 625 mK.

C, however, allows the investigation of much higher 2DEG densities. Moreover, the magnitude of the gaps is very large with the gap in device C reaching a maximum value of 625 mK, at a density of 3.35×10^{11} cm^{-2}.

One noticeable feature of the data from device C in Fig. 8 is that at the highest density measured the gap shows a pronounced drop. It has been previously reported [53] that the gap at $\nu = 5/2$ drops suddenly when the energy difference between the Fermi energy E_F and the first excited electric subband in the quantum well equals the cyclotron energy. In this case, there is a level crossing and the ground state is pushed into the lowest LL of the antisymmetric subband. Figure 9 shows the calculated [54] energy spacing along with the cyclotron energy as a function of density. As expected, the experimentally measured gap at $\nu = 5/2$ is seen to drop suddenly when the cyclotron energy becomes approximately equal to the gap between E_F and the second subband. Taken together, our calculations and experimental data indicate that larger gaps at even higher densities could potentially be achieved if the quantum well is made more narrow to further separate the ground and excited subbands.

V. CONCLUSION

To summarize, we examine the effect of heterostructure design and device processing on the performance of *in situ* back-gated 2DEGs in the second LL. We find that the position of the GaAs/AlAs superlattice barrier relative to the quantum well has a large impact on the leakage characteristics of the device due to its effectiveness in blocking the diffusion of the Ohmic contacts towards the gate and minimizing Fowler-Nordheim tunneling. Moving

the superlattice closer to the 2DEG greatly increases the range of low-leakage gating without significantly degrading the strength of the gap at $\nu = 5/2$ or other correlated states in the second LL. In addition, we find that gate-leakage dissipation powers as small as a few pW are sufficient to cause electronic heating that impacts transport in the second LL. By improving the heat sinking of the lattice, the acceptable power dissipation is increased to ~10 pW. Moreover, it is likely that the FQHE gaps would continue to rise at higher density beyond what we report here if the electric subbands were spaced sufficiently far apart. Thus, examining gaps as a function of density in narrower quantum wells could potentially yield important results on the density dependence of the gap at other states potentially useful for topological quantum computation such as $\nu = 12/5$. As we demonstrate a robust recipe for these structures and as the FQHE states in the second LL are very strong over a wide range of density, these devices should prove useful in experiments intended to test for the presence of non-Abelian statistics in quantum Hall systems.

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