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ABSTRACT

We study low-frequency charge noise in shallow GaAs/AlGaAs heterostructures using quantum point contacts as charge sensors. We observe that devices with an Al_2O_3 dielectric between the metal gates and semiconductor exhibit significantly lower charge noise than devices with only Schottky gates and no dielectric. Additionally, the devices with Schottky gates exhibit drift over time toward lower conductance, while the devices with the dielectric drift toward higher conductance. Temperature-dependent measurements suggest that in devices with Schottky gates, noise is dominated by tunneling from the gates to trap sites in the semiconductor, and when this mechanism is suppressed by inclusion of a dielectric, thermally activated hopping between trap sites becomes the dominant source of noise.

The two-dimensional electron gas (2DEG) residing in GaAs/AlGaAs heterostructures is an essential platform for exploration of mesoscopic physics.[1–3] These heterostructures are used for solid-state spin qubits[4–6] and experiments probing correlated electron states,[7,8] among many other applications. For many applications, there is strong motivation to make the 2DEG shallow while maintaining high mobility.[9–11] In surface gated devices, when the 2DEG is brought closer to the surface, the electric potential of the gates becomes more sharply defined, a beneficial attribute for mesoscopic devices requiring strong lateral confinement. However, the reduced surface-to-2DEG separation also facilitates current tunneling through the Schottky barrier, which may induce significant low-frequency charge noise.[12] Finding a means to suppress charge noise in shallow structures is essential for stable device operation.

Low-frequency charge noise is ubiquitous in low dimensional devices.[13–17] A high level of charge noise prevents stable operation of devices and can be a severe problem for many applications. Various mechanisms have been proposed to account for this form of noise. Electron tunneling from gates to trap sites in the doping layer,[13,14,16] electron hopping between trap sites within the doping layer,[18,19] and electron hopping from the doping layer to the 2DEG[20,21] have been investigated and identified as important mechanisms in gated devices. In shallow devices, tunneling may be an even more significant problem because of the thinner Schottky barrier. Several methods have been implemented to reduce the tunneling noise noise, such as bias cooling[12,13] or adding a top global gate.[14]

In this work, we use quantum point contacts (QPCs) as charge sensors to detect low-frequency charge noise in a shallow GaAs/AlGaAs heterostructure. The heterostructure is grown by molecular beam epitaxy (MBE). The layer stack is shown in Fig. 1(a) and consists of a 7 nm GaAs cap layer, a 3 nm AlGaAs barrier, a 12 nm uniformly Si-doped AlGaAs layer, a 28 nm AlGaAs spacer layer, and a 100 nm GaAs layer in which the 2DEG resides. Besides the uniformly n-doped layer, we also add a delta doping layer at the lower edge of the uniformly doped AlGaAs region (28 nm away from the 2DEG). The Al mole-fraction is 36% for all AlGaAs layers. The electron density of the 2DEG is measured to be 3.26×10^{11} cm^{-2} and the mobility is 1.6×10^6 cm^2/V s at $T = 0.3$ K. A typical device [see Fig. 1(b) inset] has split gates (5 nm Ti/10 nm Au) on the GaAs/AlGaAs heterostructure surface. For the QPCs with Schottky gates, the metal gates are deposited directly onto the GaAs surface, whereas for the QPCs with insulated gates, a 5 nm Al_2O_3 dielectric layer is deposited by Atomic Layer Deposition (ALD) between the metal gates and the surface. The Al_2O_3 is deposited on the entire area of the chip at a process temperature of

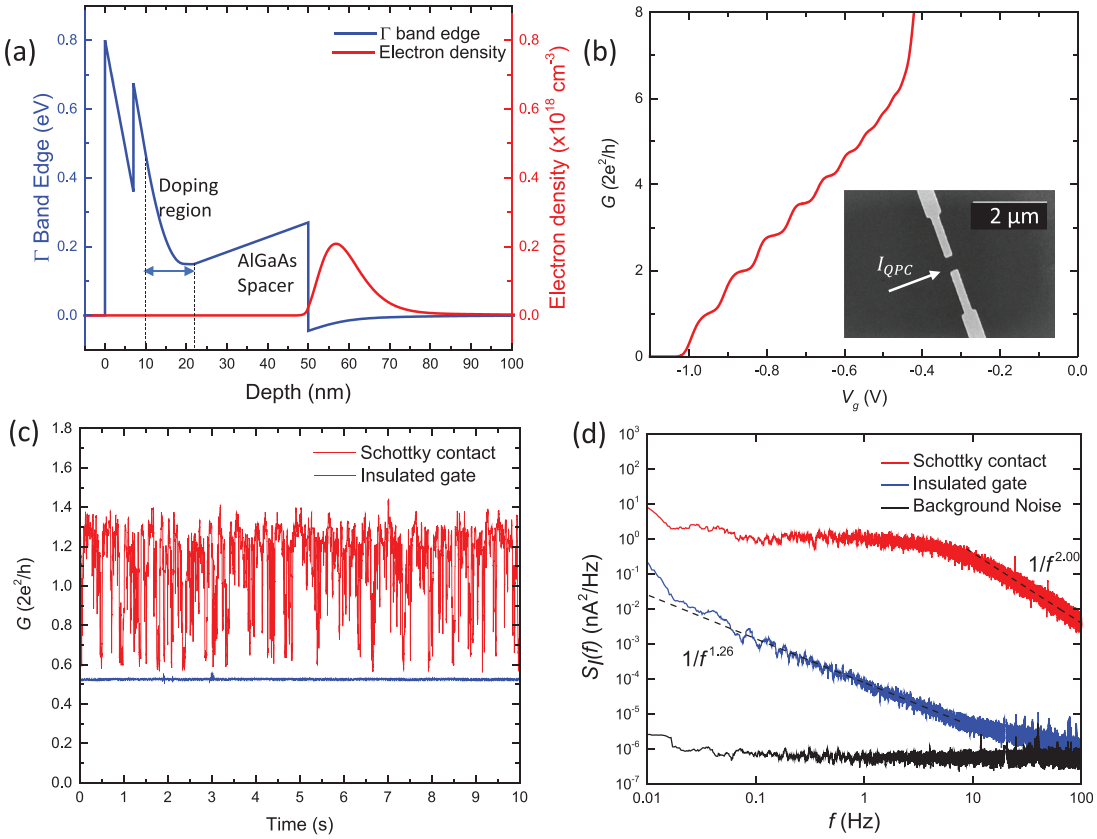

FIG. 1. (a) Simulated conduction band edge diagram at $V_g = 0$ V. (b) Conductance G of a QPC as a function of gate voltage V_g at $T = 0.3$ K. (Inset) Scanning electron microscope (SEM) image of a fabricated QPC. (c) Conductance time traces for structures with and without the dielectric layer (200 nm QPCs) at $T = 4$ K [data from the QPC with Schottky gates are offset by $0.6 \times (2e^2/h)$ for clarity]. The operating gate voltage is -0.72 V on the QPC with Schottky gates and is -0.99 V on the QPC with insulated gates. Both QPCs have been stabilized at the riser of the first plateau for 1 h prior to the measurement. (d) Noise power spectral density $S_I(f)$ derived from a FFT of the time traces, with experimental background noise $S_{I,BG}(f)$ measured at zero source-drain voltage (black trace).

200 °C. No surface pre-treatment or annealing was used. Windows in the dielectric are etched over the Ohmic contacts to enable bonding. We fabricated QPCs with gate separations ranging from 200 nm to 350 nm. Wider QPCs require more negative V_g to reach a fixed operating point of conductance, and so having multiple QPC widths enables us to determine the effect of V_g on noise. The set of QPCs with Schottky gates consisted of two 200 nm, one 250 nm, two 300 nm, and one 350 nm QPC, and the set of QPCs with insulated gates consisted of two 200 nm, two 250 nm, and two 300 nm QPCs.

We applied a voltage V_g to the two metal gates of a QPC using a Stanford Research SIM928 DC voltage source to deplete the 2DEG underneath. We used a two-terminal measurement in which a 1 kHz 200 μV AC voltage is applied to the source contact and the drain current is measured by a DL1211 current pre-amplifier. The output of the DL1211 was fed to the input of a Stanford Research SR830 lock-in amplifier. The lock-in signal was read by a National Instruments NI-DAQ digitizer. The room-temperature connections were made using BNC cables, and the low-temperature electrical wiring utilizes copper loom; no additional filters were used in the circuit. Because the excitation frequency and the frequency range of the charge noise of interest are both low, this setup provides sufficient bandwidth to avoid attenuating the signal. The cutoff frequency of the measurement is set by the time constant of the lock-in amplifier, which is set to 0.3 ms with a 24 dB per octave roll-off, corresponding to a 230 Hz cutoff frequency. A typical QPC conductance trace exhibiting quantized conductance plateau is shown in Fig. 1(b) measured at $T = 0.3$ K.

For charge noise measurements, we operate the QPCs on the riser beneath the first conductance plateau ($G_{QPC} \approx e^2/h$) where the slope $\partial G_{QPC}/\partial V_g$ is the steepest and the conductance is most sensitive to changes in the electrostatic environment due to charge noise. When electrons fill or empty the trap sites close to the QPC, the electrostatic potential changes and the conductance is modified. Therefore, fluctuations in QPC conductance can be used to probe the local charge noise. Also, we bias each QPC at the riser of the first plateau for 1 h before measuring the charge noise to avoid the conductance drift, which occurs over this time period (we discuss the drift later in this work).

Figure 1(c) shows example time traces for a QPC with a Schottky gate (red) and one with an insulated gate (blue). The red curve is very noisy, with the majority of the conductance fluctuation appearing to occur as telegraphic noise between two levels, but with significant other charge noise also visible. In the blue curve for the device with an insulating layer, the conductance variation is dramatically decreased

despite the fact that the operating gate voltage V_g is slightly more negative to maintain $G_{QPC} \approx e^2/h$.

Figure 1(d) illustrates the corresponding noise power spectral density $S_I(f)$ derived from a Fast Fourier transform (FFT) of the conductance time traces. The top curve for the Schottky gate QPC shows the Lorentzian form typical for random telegraph noise (RTN), which is flat at low frequency and drops as $1/f^2$ above the corner frequency.[22,23] The middle curve for the QPC with insulated gates exhibits noise that drops as $1/f^a$, with the exponent $a \approx 1.26$. If the RTN is eliminated, the remaining noise would be expected to have a $1/f$ power spectrum over a wide frequency range, which is characteristic of noise from an ensemble of trap sites with a homogeneous distribution of switching times.[22,24] The fact that a is slightly greater than 1 suggests that there is some remaining RTN in the QPC with insulated gates at $T = 4$ K, even though the majority is suppressed. Due to this $1/f^a$ dependence, at high frequencies the measured noise drops to the same level as the background noise, making it nearly unmeasurable.

We estimate the noise level quantitatively by calculating equivalent gate voltage noise ΔV_{EG},[14,19] which is equal to the amplitude of the voltage fluctuations that would need to be applied at the surface gates to reproduce the same conductance fluctuations as the charge noise. The expression used to calculate ΔV_{EG} is shown in Eq. (1). In this equation, $S_I(f)$ is the noise power spectral density measured for the device, while $S_{I,BG}(f)$ is the background noise power spectrum from the measurement setup,

$$\Delta V_{EG} = \sqrt{\int_{0.1}^{100} [S_I(f) - S_{I,BG}(f)]\,df} \Big/ (\partial I_{QPC}/\partial V_g). \quad (1)$$

We use $\partial I_{QPC}/\partial V_g$ to represent the sensitivity of the QPCs. We integrate the noise over the frequency range of 0.1 Hz to 100 Hz, which captures the majority of the fluctuations due to low-frequency charge noise.

Figure 2(a) shows the calculated equivalent gate voltage noise of the QPCs measured at $T = 4$ K. The most striking feature of these data is the large difference in equivalent voltage noise between the Schottky gate and insulated gate devices. While there is some device-to-device variation for the insulated gate devices, the noise level of the QPCs with insulated gates is lower by a factor of approximately 25 compared to the QPCs with Schottky gates. Since the dielectric is expected to suppress electron tunneling from the gate, the data suggest that tunneling from the gate to trap sites through the top barrier dominates

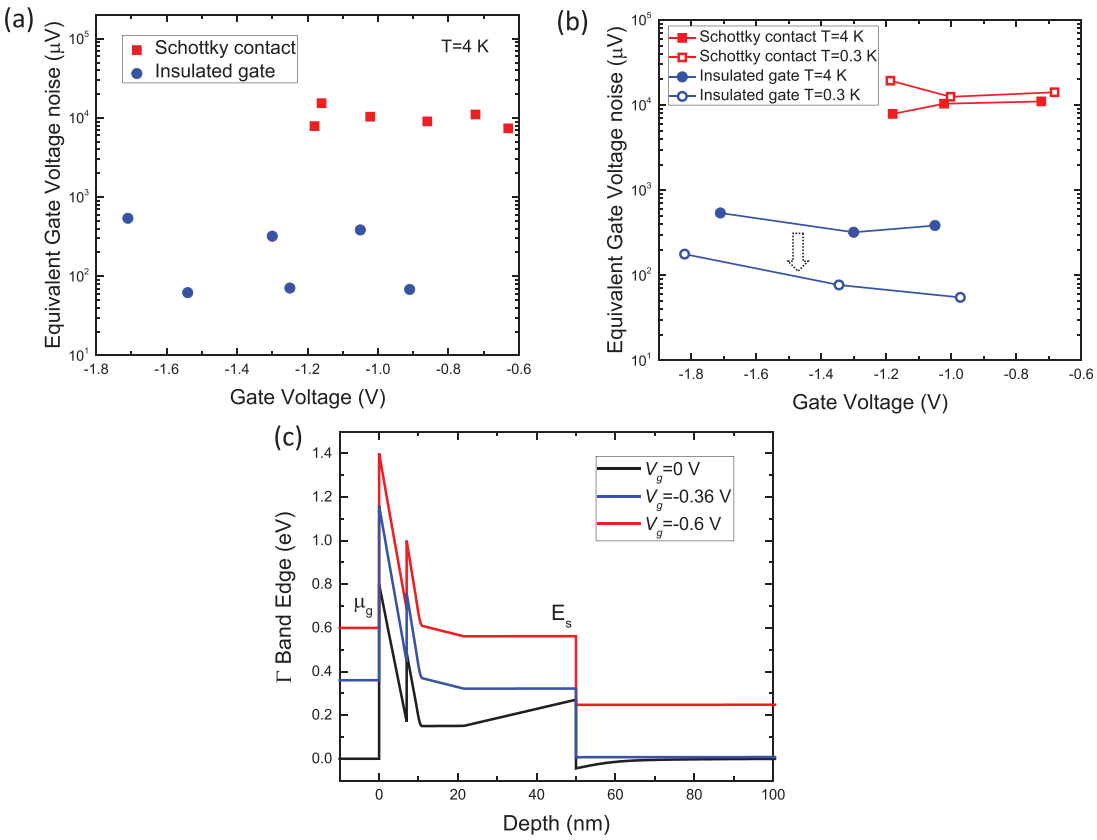

FIG. 2. (a) Equivalent gate voltage noise ΔV_{EG} of QPCs measured at $T = 4$ K. The square points represent the noise level of the QPCs with Schottky gates. The circles represent the noise level of the QPCs with insulated gates. (b) ΔV_{EG} of the QPCs measured at both 4 K and 0.3 K. Each curve shows the noise level of QPCs with different gap widths and thus different operating gate voltages. For the QPCs with insulated gates, we measured the subset of QPCs, which exhibited a higher noise level. Closed symbols correspond to measurements at $T = 4$ K and open symbols are data collected at $T = 0.3$ K. (c) Simulated conduction band edge diagram at $V_g = 0$ V, $V_g = -0.36$ V, and $V_g = -0.6$ V. The 2DEG underneath the gates is depleted at $V_g = -0.36$ V.

the noise in the QPCs with Schottky gates. These data and interpretation are consistent with previous experimental results, which have also highlighted the importance of tunneling through the Schottky barrier.[12–15,20] The second interesting aspect of these data is the weak dependence of charge noise on V_g. This behavior is different from what has been reported in previous experiments using deeper 2DEGs. Previous experiments in QPCs with 2DEGs approximately 90 nm deep have observed noise with a roughly exponential dependence on V_g.[13–15] On the other hand, measurements in FET devices using a shallow 2DEG more similar to the structure used in our experiment showed a noise that initially increased with V_g and then saturated.[12] This suggests that our QPCs with Schottky gates may be in the regime where tunneling to trap sites in the doping layer has saturated; this is plausible given the relatively high noise level observed.

To understand the weak dependence of noise on V_g in the QPCs with Schottky gates, we study in detail how V_g affects the conduction band profile. We obtain the conduction band profile by a 1D self-consistent Schrödinger–Poisson solution using the nextnano software,[25] shown in Fig. 2(c). To simplify the calculation, we utilize two delta doping layers at 10 and 22 nm depths in place of the uniform doping density.

Previous theoretical and experimental work[26,27] indicates that Si donors in the doping region may become shallow donors d^+, DX^- centers, and deep traps (which are shallower than the DX^- center). Electrons from the gate may tunnel to some of these states in the doping layer when the chemical potential of the gate μ_g meets or exceeds their energy. Figure 2(c) illustrates that the chemical potential of the surface gates μ_g is higher than the AlGaAs barrier height E_S when V_g is more negative than -0.36 V. When more negative gate voltage is applied past -0.36 V, μ_g remains at the same position relative to the doping layer; this can be seen in the red curve at $V_g = -0.6$ V. Therefore, while current will continue to leak from the gate to the trap sites in the doping layer, the contribution of this mechanism to the total leakage current will not increase when more negative voltage is applied since the energy difference between the gate and the doping region does not change. This may explain why we do not observe a significant dependence of ΔV_{EG} on gate voltage. More negative voltage should instead result in increased leakage directly to the 2DEG through the AlGaAs conduction band, which does not contribute to charge noise. Similar arguments are made in Ref. 12 to explain the saturation of noise in high electron mobility transistors.

To gain more insight into the mechanisms responsible for noise, we measured a subset of the QPCs with Schottky gates and with insulated gates at both $T = 4$ K and $T = 0.3$ K, as shown in Fig. 2(b). For the insulated gate structures, we chose to measure the subset of devices that displayed the highest noise levels at $T = 4$ K. The top two curves for the QPCs with Schottky gates exhibit noise independent of T, consistent with the picture of noise driven by tunneling from the gates, which should have little temperature dependence. Noise associated with tunneling has been found to be independent of temperature in previous experiments below 4 K.[14,20] However, in the QPCs with insulated gates, we observe a reduction in the charge noise levels by approximately a factor of 3 when temperature is lowered from $T = 4$ K to $T = 0.3$ K. This indicates that a different mechanism with a significant temperature dependence becomes relevant when the tunneling mechanism is sufficiently suppressed.

Thermally activated hopping of charge between trap sites has been proposed as a mechanism for temperature-dependent noise,[24,28] and may explain the noise we observe in the QPCs with insulated gates. In this model, for a two-level noise system (TLNS), each absorption–desorption process of an electron at a trap site gives a contribution to the noise spectrum $S_I(f, T) = \frac{\tau}{1+(2\pi f\tau)^2}$.[24,28] The switching time τ (which is the reciprocal of the corner frequency) is thermally activated such that $\tau = \tau_0 e^{E/k_B T}$.[24,28] Here, E is the activation energy and τ_0 is the characteristic attempt time of the TLNS. When the temperature decreases, the electrons are more likely to remain in the trap sites, and so the thermally activated charge fluctuations are reduced. Furthermore, the noise of an ensemble of TLNSs with a uniform distribution is expected to be proportional to $\sqrt{T}$,[28,29] which is consistent with our finding that the noise is reduced by a factor of three when T is reduced from 4 K to 300 mK. When the heterostructure is grown, the Si donors are incorporated randomly in the doping region. This will result in a disordered electrostatic potential and a wide distribution of spatial separations between pairs of donors, giving a wide distribution of effective energy barriers for electron tunneling between the donor states. Thus, it is plausible that thermal hopping between donors accounts for the temperature-dependent noise. Similar temperature-dependent noise has been observed in previous experiments in GaAs/AlGaAs heterostructures in quantum dots[29] and in QPCs.[20] Additionally, noise consistent with this thermally activated hopping mechanism has been observed in SiGe devices with Al_2O_3 dielectrics[28] and was associated with trap sites in the dielectric-semiconductor interface; this raises the possibility that hopping at this interface may also contribute to the temperature-dependent noise in our experiment. Nevertheless, it is clear that the dielectric is a significant net benefit in reducing charge noise. In the context of these previous works, our data support the existence of two major mechanisms contributing to charge noise in shallow GaAs/AlGaAs gated devices: tunneling from the gates to trap sites and thermally assisted hopping within the doping layer or dielectric-semiconductor interface.

Another feature relevant to the stability of devices is the drift of conductance over long time scales.[19] This phenomenon is illustrated in Fig. 3(a), where time traces over the first hour after initially biasing the QPCs are shown for a QPC with Schottky gates and a QPC with insulated gates. In addition to the rapid charge noise fluctuations which occur on short time scales, there is also a drift in the average conductance for both QPCs. Interestingly, the direction of this drift is different for the QPCs with Schottky gates vs those with the dielectric. For the QPC with Schottky gates, the conductance drifts down over time, while for the QPC with insulated gates, the conductance increases over time. Furthermore, this trend was consistent for all the QPCs measured. While Fig. 3(a) shows conductance at fixed gate bias, the drift results in an overall shift in the conductance vs V_g curve.[19] Therefore, a convenient way to quantify the amount of drift is by calculating how far in units of gate voltage the conductance curve shifts in 1 h (we define this drift as the shift in the gate voltage point at which the conductance drops to zero, corresponding to full pinch-off). We plot this in Fig. 3(b) for all the QPCs. The behavior of all the QPCs measured is consistent with the trend in Fig. 3(a): for the QPCs with Schottky gates, there is a positive shift in the gate voltage of the pinch off point (corresponding to a decrease in conductance at fixed V_g in the first hour), while for all the QPCs with the dielectric, there is a negative shift in the gate voltage point (corresponding to drift toward

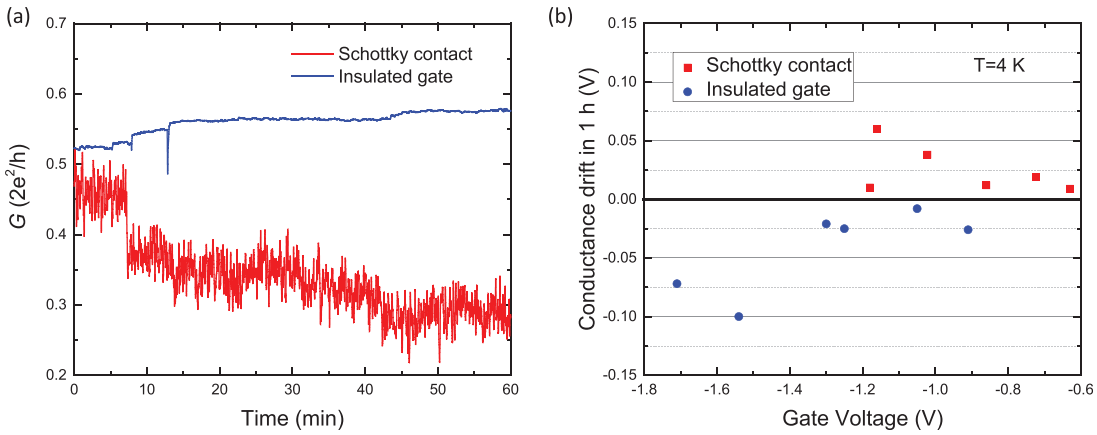

FIG. 3. (a) Conductance at a fixed V_G vs time. The red curve is measured on a QPC with Schottky gates initially biased at the riser of the first conductance plateau. The blue curve is measured on a QPC with insulated gates. (b) Shift in the pinch-off voltage due to the QPC drift after 1 h measured at $T = 4$ K. The red square points are measured from QPCs with Schottky gates, and the blue circles are measured on QPCs with insulated gates.

increased conductance). Clearly, the dielectric must have a significant impact on the mechanism behind the conductance drift. Additionally, for both sets of QPCs, there is a trend toward increased drift amplitude with more negative operating gate voltage.

A mechanism behind conductance drift in devices with Schottky gates is discussed in Ref. 19. According to this model, since electron tunneling in the QPCs with Schottky gates can be significant, charge can be easily transferred from the metal gates to the doping layer. Hence, it is likely that the chemical potential at the doping layer tends to equilibrate with the energy level of the Schottky gates. When negative voltage is applied to the gate, some available states in the doping layer drop below μ_g and become filled. The accumulated electrons in these states result in a negative electrostatic potential felt by the 2DEG, which is equivalent to more negative gate voltage. Therefore, conductance decreases over time and the gate voltage required to pinch off the QPCs becomes less negative.

The situation is different for devices with insulated gates. The Al_2O_3 dielectric layer has a high band edge,[30] which strongly suppresses charge tunneling between the gates and the doping layer. Hence, states in the doping layer cannot equilibrate with μ_g. The negatively biased metal gates simply repel the electrons which are already in the doping layer, tending to deplete these electrons over time. As electrons are depleted from these states, the negative electrostatic potential experienced by the 2DEG is reduced, leading to increased QPC conductance over time and a negative shift in the pinch-off voltage.

In conclusion, our measurements suggest that there are two distinct mechanisms behind charge noise in gated shallow GaAs/AlGaAs heterostructures. In QPCs with Schottky gates, noise is dominated by the leakage of electrons from surface gates to the states in the doping region. Adding a 5 nm Al_2O_3 dielectric layer between the gates and the semiconductor surface suppresses the tunneling noise. After this tunneling mechanism is suppressed, a thermally activated noise mechanism dominates the noise, and this noise has a significantly smaller amplitude compared to the tunneling noise. The dielectric enables reasonably stable operation of shallow heterostructures, which would otherwise suffer from the excessive noise. Finally, we observe that although both types of QPCs exhibit conductance drift over time, QPCs with Schottky gates drift toward lower conductance while QPCs with insulated gates drift toward higher conductance, and this difference may be explained by equilibration with the gate and suppression of tunneling, respectively. This work informs improvements in device stability and points toward the possibility of using shallow GaAs 2DEGs for spin qubits and other mesoscopic devices.

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DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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