ARTICLES
https://doi.org/10.1038/s41928-020-00528-y

nature electronics

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A cryogenic CMOS chip for generating control signals for multiple qubits

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Scaled-up quantum computers will require control interfaces capable of the manipulation and readout of large numbers of qubits, which usually operate at millikelvin temperatures. Advanced complementary metal–oxide–semiconductor (CMOS) technology is an attractive platform for delivering such interfaces. However, this approach is generally discounted due to its high power dissipation, which can lead to the heating of fragile qubits. Here we report a CMOS-based platform that can provide multiple electrical signals for the control of qubits at 100 mK. We demonstrate a chip that is configured by digital input signals at room temperature and uses on-chip circuit cells that are based on switched capacitors to generate static and dynamic voltages for the parallel control of qubits. We use our CMOS chip to bias a quantum dot device and to switch the conductance of a quantum dot via voltage pulses generated on the chip. Based on measurements from six cells, we determine the average power dissipation for generating control pulses of 100 mV to be 18 nW per cell. We estimate that a scaled-up system containing a thousand cells could be cooled by a commercially available dilution refrigerator.

Quantum computing is expected to offer a computational advantage over classical computers in several applications that could be used to solve a variety of important problems[1–5]. However, a useful quantum computer will require a large number of high-fidelity qubits and a control interface[6–14] that passes signals between the classical (usually at room temperature) and quantum (usually at cryogenic temperatures) domains of the system (Fig. 1a). Unlike classical processors, quantum circuits cannot fan-in and fan-out data[15,16] and thus face a significant input–output bottleneck[17]. In particular, every qubit in a quantum computer is individually controlled by external circuitry[7,9,18], which adds noise and heat to the qubit system[19]. Brute-force approaches to manage these signals—via the use of individual components per qubit—limits the scaling potential of these systems[16]. This challenge is illustrated by the recent state-of-the-art experiment that required around 200 wideband coaxial cables, 45 bulky microwave circulators and racks of room-temperature electronics to control 53 qubits (ref. [20]).

In this Article, we report a chip-based cryogenic complementary metal–oxide–semiconductor (CMOS) interface system that can generate control pulses for multiple qubits at 100 mK. Our approach is based on a CMOS chip that has ultralow power dissipation and achieves tight integration between the qubits and their control circuits. Our architecture does not require the monolithic integration of the control system and qubits on the same substrate[21], and it does not require individual electrical connections from room temperature (or 4 K) to every qubit[11,13]. Instead, our architecture makes use of chip-to-chip interconnects[22] to manage the input–output bottleneck and could potentially be compatible with various semiconductor-based qubit platforms, including those based on Majorana zero modes (MZMs)[23], electron spins[24] or gatemon devices[25].

Our CMOS chip is a 2.5 mm × 2.5 mm integrated circuit with around 100,000 transistors. A serial peripheral interface (SPI), which consists of four low-bandwidth wires connected at room temperature, is used to provide the digital instructions (input signals) to the chip. These input signals are handled by the digital logic of an on-chip finite-state machine (FSM), which then configures 32 analogue circuit blocks, each of which can be used to control a single gate of a qubit. These analogue circuit blocks—termed charge-lock fast-gate (CLFG) cells—use the low leakage of the transistors at cryogenic temperatures to store and shuffle charge between the floating capacitors to generate the dynamic voltage signals for manipulating qubits. Compared with a direct connection to room temperature or 4 K via a cable[11,14], moving the stored charge between small, on-chip capacitors consumes significantly less power[23,24] and has a smaller footprint of 100 μm × 100 μm for a single CLFG cell. We benchmark this architecture on a GaAs few-electron quantum dot (QD) device[26] and measure the charge leakage and power dissipation under various operating regimes. We then use these results to project the feasibility of scaling up the approach. This suggests that complex circuits based on modern CMOS technology can be designed to operate near 100 mK and can potentially provide a scalable platform for controlling the large number of qubits needed to realize quantum applications.

Architecture

In our setup, the CMOS control chip is placed between the qubits and room-temperature electronics. The full stack of elements needed for quantum computing is shown in Fig. 1a,b. The cryo-CMOS chip is tightly packaged with a QD test platform (Fig. 1c), which is also wire bonded to a chip that contains superconducting resonators for frequency-multiplexed readout[27]. The generic platform based on GaAs QDs and resonator structures, which serves as a stand in for

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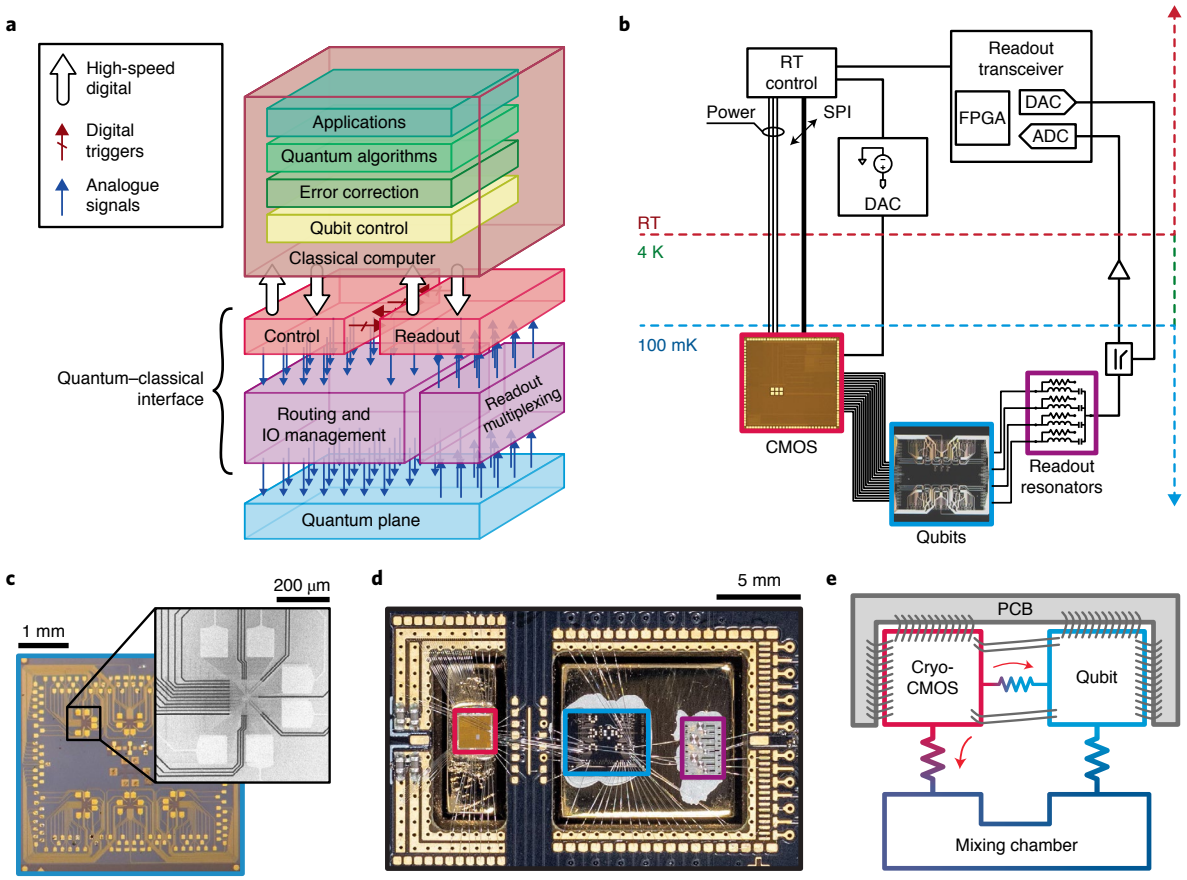

Fig. 1 | The quantum–classical interface of a quantum computer. a, The generic stack of elements needed for quantum computing. **b**, Control and readout sub-systems, distributed between room temperature (RT) and 100 mK. A readout transceiver with integrated field-programmable gate array (FPGA), digital-to-analogue converter (DAC) and analogue-to-digital converter (ADC) is used to readout multiple qubits at once. The cryo-CMOS (brown) chip addresses the input–output (IO) bottleneck for control signals. **c**, Photograph and electron micrograph of our qubit test platform based on GaAs QDs (see Methods for details). **d**, Photograph showing the cryo-CMOS chip (red box), qubit test chip (blue box) and resonator chip (purple box). Each chip is anchored onto a gold-plated copper thermalization pillar, with a separate pillar used for the CMOS chip. **e**, Simplified thermal conductance model of the setup. The intended use of the partially separate cooling pillars is to increase the thermal conductivity to the mixing chamber (big red arrow) while reducing the direct heat (little red arrow) flowing from the hot CMOS chip to the qubit devices.

the various possible qubit platforms, offers fast and sensitive measurement of the performance of the CMOS control chip at 100 mK. To mitigate unwanted heating of the quantum devices, each chip is bonded with silver paste to partially separated gold-plated copper pillars that are in parallel thermal contact with the mixing-chamber stage of a dilution refrigerator (Fig. 1d). This arrangement is used to reduce the direct heat flow from the CMOS circuits to the qubit chip (Fig. 1e). A custom printed circuit board (PCB) and wire bonds form the electrical connection between the chips. We note that the carriers internal to the CMOS devices can be out of equilibrium and exhibit an effective temperature that is larger than the lattice temperature.

The control chip is implemented in 28 nm fully depleted silicon-on-insulator technology—a low-power and low-leakage CMOS platform that is well suited for cryogenic operation[28–30] (further process details are provided in Supplementary Information Section 1). Transistors in this technology have the utility of configuring a back-gate bias to offset changes in the threshold voltage with temperature. This process provides both high-voltage (1.8 V) and low-voltage (1.0 V) devices and also allows for individual back-gate control of both *n*- and *p*-type transistors or entire circuit blocks, a useful aspect in mixed-signal circuit design such as our control system.

CMOS control chip

The floor plan of our CMOS chip is shown in Fig. 2a and comprises both digital and analogue blocks. In the lower left corner of the chip, digital circuit blocks provide communication, waveform memory and autonomous operation of the chip via an FSM (~100,000 transistors). The memory is configured as a 128-bit register, allowing an arbitrary pulse pattern to be stored. A master oscillator is also included, implemented as a ring oscillator with a configurable output frequency. Tiled along the left and bottom edge of the chip is a repeating analogue circuit block (CLFG) that generates the static and dynamic voltages needed for controlling the qubits. In the prototype described here, 32 CLFG cells are realized on a single die, enabling connection to 32 qubit-control electrodes (a detailed description of the circuit blocks is provided in the Supplementary Information).

The basic functionality of a CLFG cell is captured by the circuit shown in Fig. 2b. The circuit incorporates an on-chip capacitor $C_{PULSE,N}$, part of each CLFG cell, while $C_{P,N}$ in the diagram represents the parasitic capacitance arising from the bond pad, bond wire and gate interconnect on the qubit chip. The voltage V_{HOLD} is defined by a room-temperature digital-to-analogue converter (DAC). An individual cell is selected for configuration by the on-chip FSM, which connects the output terminal of the cell to the external voltage

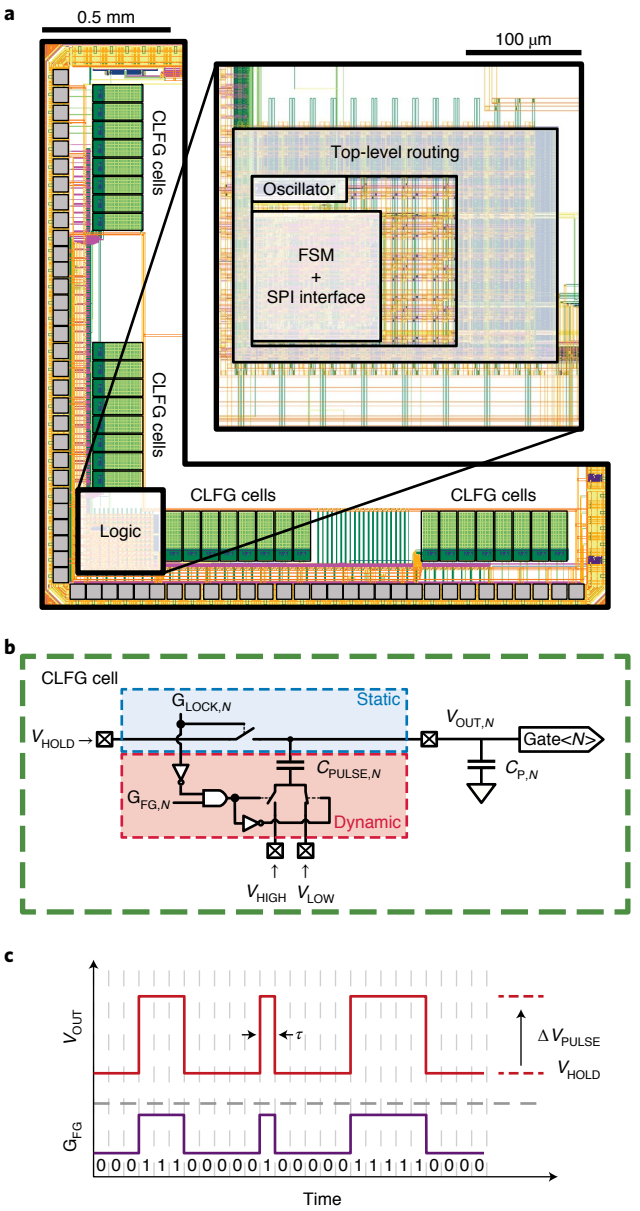

Fig. 2 | Corner floor plan and operation of the CMOS control chip. **a**, Location of the digital logic blocks (inset shows a zoomed-in image of the block in the lower left corner). Tiled around the left and lower edge of the chip are 32 cells termed the CLFG. These analogue blocks generate static and dynamic voltages at their output (grey squares denote the bond pads). **b**, Schematic of a single CLFG cell, where $C_{P,N}$ is the sum of the parasitic capacitances due to interconnect wiring on the CMOS and qubit chips. $C_{PULSE,N}$ is the on-chip capacitor. The d.c. charge locking takes precedence over the fast gating action, that is, whenever $G_{LOCK,N}$ is V_{HIGH}, $G_{FG,N}$ is ignored and the bottom plate of $C_{PULSE,N}$ connects to V_{LOW}. **c**, Output voltage of the cell as $G_{FG,N}$ is pulsed, assuming a voltage V_{HOLD} is locked on the cell. τ is the minimum pulse duration, set by the period of the CLFG clock.

source by closing the switch $G_{LOCK,N}$, thereby setting $V_{OUT,N} = V_{HOLD}$. This charges the capacitors required to maintain a static voltage at the high-impedance output. Following the charge up, the switch $G_{LOCK,N}$ is opened by the FSM, leaving the charge on the capacitors and qubit gate floating. The low transistor leakage at low temperature allows the charge to be locked for a reasonable time even as the CLFG cell is de-selected, establishing a static voltage at the output. Through sequential cell selection and appropriate adjustment of V_{HOLD}, the single input voltage source can be multiplexed to configure the required voltage biases of many qubit gates.

For dynamic control, a voltage pulse is required to rapidly change the energy state of the qubit[24,25]. Schemes based on MZMs manipulate the qubit via measurement but additionally require large (~100 mV) voltage pulses to open and close the tunnel barriers in a specified sequence[23]. Generating such a pulse with electronics that is significantly decoupled from the qubit plane requires the use of cables, for instance, that run from the millikelvin stage of the refrigerator to 4 K or room temperature. Driving the impedance of such cables and their attenuators can result in significant power dissipation inside the refrigerator, even if no power is dissipated at the end of the open line. Alternatively, by tightly integrating the qubit plane and controller, a sizable voltage pulse can be generated with little energy by the redistribution of local charge in a circuit with small capacitance (and high impedance). We exploit this concept in the dynamic operation of the CLFG cell to generate pulses at $V_{OUT,N}$. The FSM can be programmed to enable the selected cells for pulsing and delivering a pre-loaded pulse pattern to the switch $G_{FG,N}$, as shown in Fig. 2c. The function of the switch is to toggle the potential of the lower plate of the capacitor $C_{PULSE,N}$ between the two voltage sources V_{HIGH} and V_{LOW}. With the potential of the lower plate of $C_{PULSE,N}$ switched to V_{LOW} or V_{HIGH}, charge is induced on the top plate, changing the output voltage $V_{OUT,N}$ that is seen at the qubit gate with respect to the ground. The magnitude of the pulse is given by

$$\Delta V_{PULSE,N} = \frac{C_{PULSE,N}}{C_{P,N} + C_{PULSE,N}}(V_{HIGH} - V_{LOW}) \quad (1)$$

Note that by toggling between two voltage sources at 100 mK, as opposed to the standard method of pulsing from room temperature, we avoid the need to charge or discharge the capacitance of the cables that run from room temperature down to the qubit plane. Thus, it is only the capacitance in the charge-shuffling circuit that contributes to the power dissipated:

$$P_{PULSE} = \frac{C_{PULSE,N}C_{P,N}}{C_{P,N} + C_{PULSE,N}}(V_{HIGH} - V_{LOW})^2 f \quad (2)$$

where f is the pulse frequency. Importantly, as $C_{P,N}$ and $C_{PULSE,N}$ are picofarad capacitances, they require very little power to charge (as measured below).

Performance benchmark

We now benchmark the performance of our CMOS controller using a GaAs-based QD device (see Methods for device and measurement details). Select gates on the QD device are bonded to the output pads of the CLFG cells on the CMOS chip, as indicated by the switched connections shown at the bottom of Fig. 3a. In order to compare the performance of the CMOS circuits to standard control approaches, we also connect some of the gates that define the QD to lines directly biased by a room-temperature DAC (Fig. 3a). Depending on the combination of the gates used, our device[26] can be configured to form QDs in various locations as indicated by the red and green ovals in Fig. 3a. As a basic demonstration of multiplexing through charge locking, we programme four CLFG cells to bias four gates, using a single external voltage source, to create the QD shown in red (Fig. 3a). The current transported through this dot, as a function of V_{LP} (also routed through the 5th CLFG cell), exhibits familiar Coulomb blockade oscillations, as shown in Fig. 3b.

A second QD, as shown in green in Fig. 3a, is also configured in the same device to measure the leakage of CLFG cells, with transport data shown in the inset of Fig. 3b for the case where V_{LW} is locked and V_{SDP} is swept (see Fig. 3a for the gate labels). Biasing this dot to the edge of a Coulomb blockade peak and measuring the transport current as a function of time allows charge leakage from

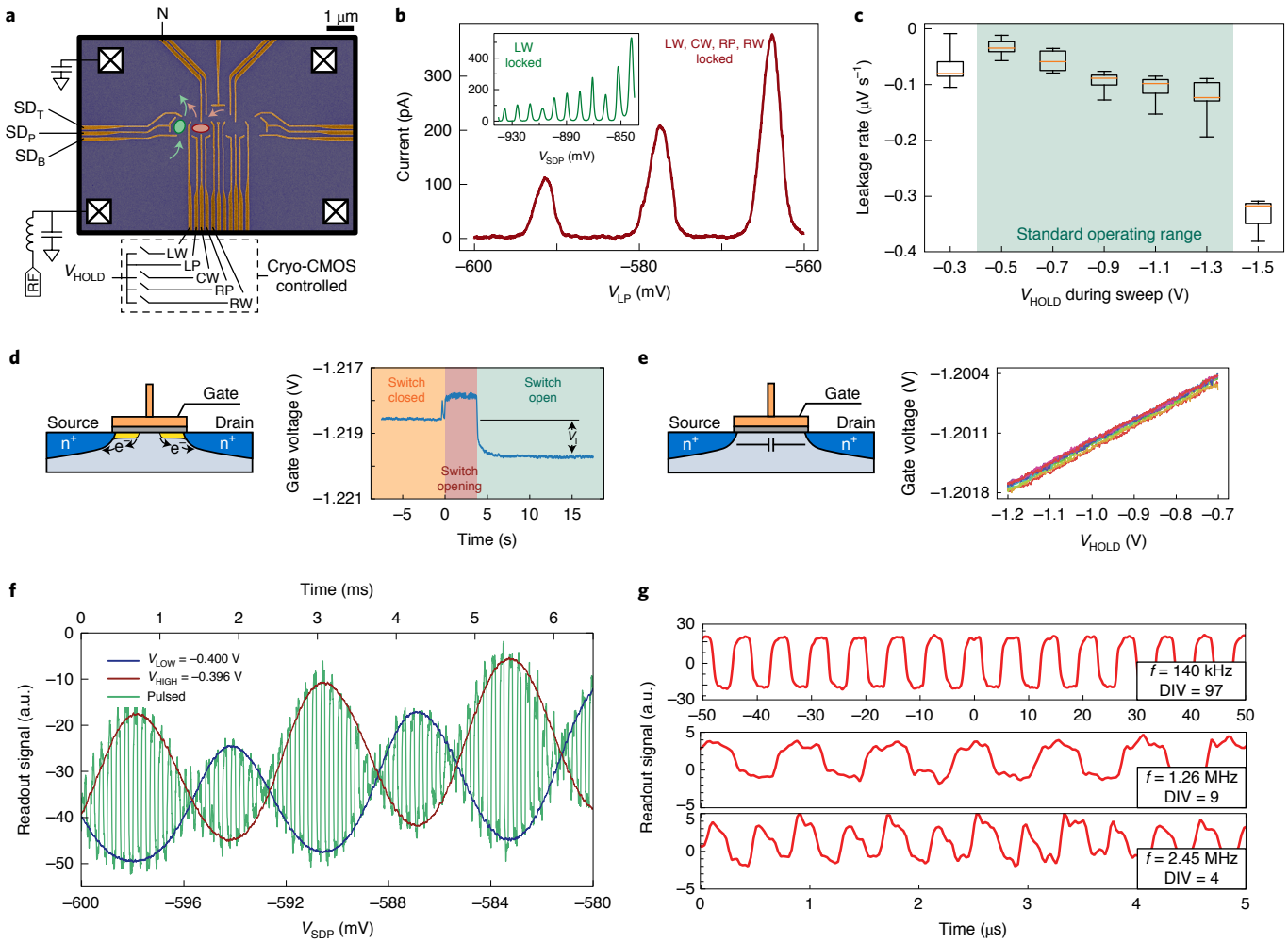

Fig. 3 | Benchmarking the cryo-CMOS control with a QD chip. a, False-colour scanning electron micrograph image of the active area of the QD device. Contacts to the reservoirs are schematically shown as black crosses. Gates used to form QDs are labelled LW, LP, CW, RP, RW, N, SD_T, SD_P and SD_B (red and green ovals indicate the QDs), and current paths used to probe the dots are shown with arrows for each QD. LW, left wall; LP, left plunger; CW, centre wall; RP, right plunger; RW, right wall; N, nose; SD_T, sensing dot top; SD_P, sensing dot plunger; SD_B, sensing dot bottom. **b**, Single-electron tunnelling through the red QD when four gates are charge locked by the CLFG cells (V_{LP} is the voltage swept during the measurement). The inset shows a QD (green) where one gate is charge locked and the other gate is varied with a room-temperature DAC. **c**, Leakage rate of the voltage held on a gate, after $G_{LOCK,N}$ is opened and V_{HOLD} changes (error bars and statistical analysis are described in the Methods, and related measurements are given in Extended Data Figs. 1–3). **d**, Output gate voltage as $G_{LOCK,N}$ is opened. An offset (V_i) between the pre-locked and locked voltage is observed due to the charge injected from the transistor channel to the gate capacitance. The switch-opening time (shaded red) is the period during which digital communication occurs. The decay in the gate voltage after the switch is opened is induced by the large *RC* time constant of the transport measurement rather than the response of the gate. **e**, Output gate voltage as V_{HOLD} is swept with the switch open. A reversible change in the locked voltage is observed due to the parasitic source–drain capacitance of the hold switch. **f**, Readout signal (voltage produced by the demodulated radio-frequency reflectometry proportional to conductance) through the green QD when the output voltage is referred to V_{LOW} (blue), V_{HIGH} (red) and when the switch is rapidly pulsed by the fast gating circuit (green), while V_{SDP} is swept rapidly. The equivalent time is shown along the top axis. For each trace, the voltage on the LW gate is locked at −1.1 V. **g**, Increasing the frequency of the square-wave pulses using the internal frequency divider with division DIV, connected to the integrated ring oscillator.

the CLFG cell to be directly detected, essentially using the auxiliary dot as a calibrated sensor of the gate voltage. The charge leakage leads to the voltage on the gate changing (deterministically) at a rate of one part in 10^7 per second (hundreds of microvolts per hour) and is dependent on the value of V_{HOLD}, as shown in Fig. 3c. This leakage rate is sufficiently low to enable a 'round-robin' refresh cycle every few minutes to lock and stabilize many gates with a single DAC input to the control chip. Decreasing the leakage further is possible by increasing the capacitance of the CLFG cell, at the expense of the pulse rise time and chip footprint.

Measurements of the QD conductance, as shown in Fig. 3d, also provide a means of monitoring the charge-locking process, including charge injection at the CMOS switch, which pushes additional charge onto the gate capacitance as the switch is opened (Fig. 3d). There is also a linear offset in the gate voltage that depends on the value of V_{HOLD}, as shown in Fig. 3e. This offset comes from the charge induced on the gate via the transistor capacitance when the switch is open. In our setup, both charge injection and linear offset effects are calibrated and transparently accounted for in software that interfaces with the control chip.

Our QD structure can also be configured as a radio-frequency single-electron transistor by embedding it in an impedance-matching *LC* tank circuit[31], an aspect that allows the detection of the gate-pulsing action of the CMOS chip with a

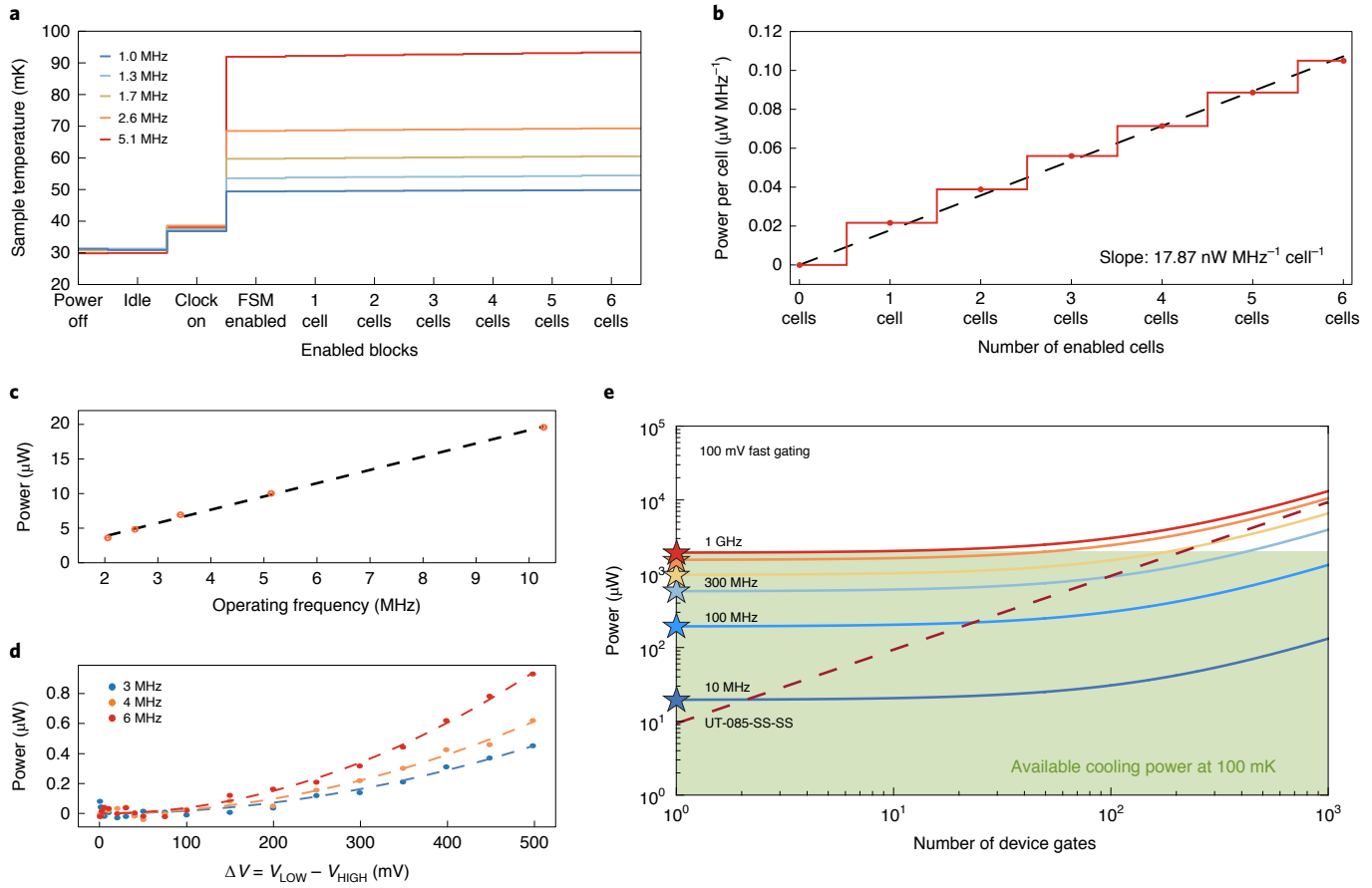

Fig. 4 | Power dissipated at 100 mK when interfacing with the QD device. a, Temperature of the system for various operating modes of the cryo-CMOS chip. The steady-state temperature progressively increases as the on-chip clock and FSM block are enabled, followed by simultaneous fast pulsing on 1 to 6 output gates in sequence. **b**, Calibrated incremental power generated by cryo-CMOS while applying 0.1 V pulsing on each qubit gate using CLFG cells 1–6. We extract the average heat cost to be 18 nW MHz^{-1} $cell^{-1}$. Each sub-system in the cryo-CMOS control integrated circuit is measured in isolation and its heat load is characterized. **c**,**d**, Power dissipated by the FSM block for different operating frequencies (**c**) and plots of the measured $C\Delta V^2 f$ power for different fast gating frequencies and amplitudes (**d**). **e**, Projected total system power of the cryo-CMOS controller generating 100 mV pulses, as a function of the number of qubit gates and operating frequency, based on the measured power dissipation. The frequencies are 10 MHz, 100 MHz, 300 MHz, 500 MHz, 800 MHz and 1 GHz. Stars on the left-hand side of the plot indicate the one-off power required for the digital circuit blocks, independent of the gate count. The green-shaded region indicates the cooling power that is achievable with today's commercial dilution refrigerators while keeping the qubits at 100 mK. The red dashed line shows the effective power dissipated in a standard coaxial transmission line of the kind commonlyused for qubit control (UT-085-SS-SS with 3 dB attenuation).

bandwidth of ~10 MHz. As a first demonstration, we programme the cryo-CMOS chip to charge lock the gate electrodes and switch $G_{FG,N}$ at 140 kHz. The CLFG voltage pulse amplitude is calibrated to switch the dot conductance from the top of a Coulomb peak to a trough. Simultaneously sweeping a second gate voltage (V_{SDP}), we observe the modulation of dot conductance whose envelope maps out the Coulomb blockade oscillations, as shown by the green trace in Fig. 3f. The envelope overlaps with the red and blue traces in the figure, which corresponds to the direct measurement of the oscillations by setting V_{HIGH} or V_{LOW} and sweeping V_{SDP} without pulsing, thus verifying the action of the CMOS pulsing circuit. Disabling the V_{SDP} sweep, we bias the device to directly observe the conductance modulation as a continuous square wave. The CMOS oscillator circuit can also be configured to modify the frequency of the pulses, as shown in Fig. 3g. Note that the apparent rise time of these pulses is limited by the bandwidth of the *LC* tank circuit. The true rise time, set by the *RC* constant of the CMOS switches and total capacitance, is of the order of a few nanoseconds. Beyond verifying the action of the CMOS pulsing circuit, these results demonstrate the suitability of the controller for manipulating single-electron states by rapidly varying the chemical potential of a device as required for qubit control.

We also measure the temperature of the packaged system as each circuit block in our control chip is powered up sequentially, as shown in Fig. 4a. Separating the contributions arising from the clock generator, FSM and CLFG cells (including $C_{PULSE,N}$ and $C_{P,N}$), the data in Fig. 4a show that the temperature remains below 100 mK for frequencies of the order of a few megahertz. In our setup, the temperature is measured by a thermometer in close proximity to the qubit chip and is significantly higher than the temperature measured by a second thermometer at the mixing-chamber stage of the refrigerator (96 mK compared with 36 mK when running at 5.1 MHz). The presence of such a thermal gradient suggests that lower temperatures are possible with improved packaging that achieves better thermalization of the chips to the refrigerator.

These temperature measurements can then be used to indicate the power dissipated by each CMOS circuit block, with nanowatt precision. To measure the dissipation, we first record the temperature of the thermometer as a function of heat applied to a resistor inside the CMOS chip with a known resistance and measured

voltage bias. This provides a conversion between the on-chip power dissipation and temperature (see Methods for further details). For the purpose of extrapolating our results to larger numbers of control lines, we determine the power of each block, showing the independent contribution from the CLFG cells (Fig. 4b) and FSM (Fig. 4c). We observe the expected quadratic dependence of the power with gate voltage amplitude, as shown in Fig. 4d. Note that our method for determining power dissipation with nanowatt precision via the calibrated measurement of small changes in the temperature is consistent with the coarse estimates of dissipation obtained by measuring the power supplied to the chip.

Combining these results, the total system power can then be determined as a function of frequency and the number of output gates. Figure 4e shows the projected total system power for a cryo-CMOS controller generating pulses with 100 mV amplitude (needed for controlling the MZM qubits). The green-shaded region indicates the cooling power provided by commercially available dilution refrigerators (Leiden Cryogenics Dry Dilution refrigerator, CF-2500). As a comparison, we also plot the effective power dissipated in a standard coaxial transmission line of the kind commonly used for qubit control (UT-085-SS-SS with 3 dB attenuation)[19]. Given that for qubits based on MZMs, the clock speed of quantum logic gates is a few megahertz (ref. [23]), it appears (Fig. 4e) that the CMOS-based control of thousands of qubits could be a viable approach.

Conclusions

We have developed a CMOS chip that can generate control signals for multiple qubits at cryogenic temperatures. Our approach provides a power-efficient interface between room-temperature electronics and QDs at 100 mK. The approach could also be potentially compatible with alternative qubit platforms based on electron spins or gatemons[25]. In such systems, the CMOS circuits could either provide direct control[24] or be configured to use the output of the CLFG cells to pulse a gate that brings the qubit into resonance with a microwave tone. These circuits could also be combined with a cryogenic switch matrix[8], to steer microwave pulses to the appropriate qubit under the control of our CMOS platform. For a scaled-up implementation of our cryo-CMOS chip, we estimate the footprint of 1,000 CLFG cells to occupy an area of a few square centimetres, which is compatible with conventional CMOS fabrication. However, further advances in the scaling of quantum gates, as well as qubit control, will be required to enable the control of a large number of qubits.

Methods

QD fabrication and measurement. The QD device was formed in a two-dimensional electron gas located 91 nm below the surface of a GaAs/(Al,Ga)As heterostructure. The density and mobility were measured using Hall bar geometry as 1.89×10^{11} cm^{-2} and 4.6×10^{6} cm^2 (V s)$^{-1}$, respectively. Contact was made to the two-dimensional electron gas using NiGeAu ohmics and annealing was performed at 450 °C for 150 s. An 8 nm Al_2O_3 dielectric is deposited via atomic layer deposition at 200 °C and is used to separate the TiAu surface gates from the heterostructure and allow the application of positive voltages without gate leakage. The gate layout used to form the QDs is described in detail in ref. [26].

Measurements are performed in a dilution refrigerator with a base temperature of 10 mK. The device is cooled with a positive bias of 100 mV to reduce the effects of charge noise in the donor layer of the heterostructure. The electron temperature was measured to be 60 mK at the base temperature of the refrigerator with the cryo-CMOS turned off. The d.c. readout is performed using standard lock-in techniques with an excitation between 10 and 50 μV. To obtain the time-domain traces (Fig. 3f,g), a high-bandwidth readout is performed via radio-frequency reflectometry[31] with a resonator attached to the bottom left ohmic contact (as shown in Fig. 3a). The bandwidth of the resonator is designed to be 10 MHz, and it limits the direct measurement of the rise time for fast gating.

Analysis of leakage rates. To analyse the leakage rates of a gate controlled by our cryo-CMOS, we use a quantum point contact (QPC) formed using the LW gate and the SD_T gates of the QD. Extended Data Fig. 1a shows that only the LW gate is controlled by our cryo-CMOS chip, such that we can focus our measurement to a single gate. To extract the voltage stored on the gates, a calibration curve is first obtained while the switch $G_{LOCK,N}$ is closed, which allows us to find the mapping between the current through the QPC and the voltage on the charge-locked gate. A sample of such a trace is shown in Extended Data Fig. 1b.

To extract the leakage rate, the left-wall voltage is set such that the sensitivity of the QPC is maximized, that is, at the midpoint of the final plateau, and the charge-locking switch $G_{LOCK,N}$ is opened, taking into account the effects of charge injection and source–drain capacitance (Fig. 3d,e). The current through the QPC is then monitored over time (Extended Data Fig. 1c) and converted back into a voltage stored on the LW gate (Extended Data Fig. 1d). Over the course of long measurements, the effects of low-frequency charge noise must be taken into account, which causes jumps in the current flowing through the QPC[32]. Raw traces showing such jumps at different values of V_{HOLD} are shown in Extended Data Fig. 2. To prevent these jumps from affecting the measured leakage rate, they are identified using a matched filter looking for steps over a length of 20 s, and the data are split at each jump. Then, to extract a leakage rate, linear fits are performed on each segment of the processed data. The results of this extraction is shown in Extended Data Fig. 3.

As the leakage is expected to vary as a function of the source–drain voltage (V_{SD}) and the source–gate voltage (V_{SG}) of the charge-locking switch, the value of V_{HOLD} is varied in steps of 0.2 V once the switch is opened. Each measurement is repeated for a total of three to four times to gather statistics on the leakage rate. The data before any processing are shown in Extended Data Fig. 2; data after the removal of charge noise are shown in Extended Data Fig. 3 for each value of V_{HOLD} measured.

Extrapolation of heat load. To extrapolate the heat load of our measurement setup when scaled to thousands of qubits, we extract the power dissipated by each component of the circuit. This includes the individual circuit elements on our cryo-CMOS chip and the power dissipated due to the capacitance of the gate. To extract the power dissipated by the cryo-CMOS chip, a calibration between the temperature of a thermometer mounted on the sample PCB and the power dissipation on the chip is obtained by passing the current through a known resistance on the chip, up to 40 μW, in nine power steps. By using an on-chip resistance, we exclude the effects of any thermal gradient between the thermometer and the chip due to bad thermal contact or due to the relative location of the mixing chamber, thermometer and cryo-CMOS chip. The temperature of the thermometer is then used to extract the power dissipated by each component as they are sequentially powered on.

Looking first at the elements of the cryo-CMOS chip, we separate the components that are shared between all the gates, namely, the oscillator and FSM (including the waveform memory), and the components that are duplicated for each gate, termed the CLFG cells. Each of these elements dissipates power due to $CV^2_{LOGIC}f$ dissipation, where V_{LOGIC} is a constant and set by the power supply voltage of the CMOS chip. We emphasize that the power dissipation due to the CLFG cells is caused by the switching action of the CMOS switches that make up the cell. The dissipation from the applied pulses is considered separately below. To isolate only the dissipation of the CLFG cell, we set $V_{HIGH}=V_{LOW}$ such that the pulse amplitude (ΔV_{PULSE}) is zero. The dissipation of each of these elements is extracted by sequentially powering up individual elements and sweeping the operating frequency of the chip. From this, we find $P_{OSC}=0.28\times10^{-6}$ W MHz^{-1}, $P_{FSM}=1.92\times10^{-6}$ W MHz^{-1} and $P_{CLFG}=N\times11.23\times10^{-9}$ W MHz^{-1}.

In addition to the heating of the logic cells on the cryo-CMOS chip, additional power is consumed due to the CV^2f dissipation at the gate, which is given in equation (2).

To extract this capacitance and hence the power dissipated at the gate, the voltage difference between V_{HIGH} and V_{LOW} is swept. From this, an equivalent capacitance of $C_{EQUIV}=1.05$ pF is extracted, which comprises the on-chip pulsing capacitor $C_{PULSE}=5.60$ pF and a parasitic capacitance, which we extract using the known pulsing capacitance, as $C_P=1.29$ pF.

Using these values, the curves in Fig. 4e are calculated using the following equation:

$$P_{CMOS}(\Delta V_{PULSE}, f, N) = fP_{OSC} + fP_{FSM} + Nf\left(P_{CLFG} + \Delta V^2_{PULSE}C_{EQUIV}\right) \quad (3)$$

where f is the operating frequency and N is the number of gates controlled by the circuit.

The comparison to a standard coaxial cable is made assuming a stainless steel coaxial cable (UT-085-SS-SS) and using 3 dB attenuation at the mixing chamber, which is necessary for filtering and thermalization of the inner coaxial line[19]. This leads to static dissipation due to the thermal conduction of the coaxial cable, which we consider to be 13.6×10^{-9} W, as well as the dissipation of the incoming signal in the attenuator. We note that the use of superconducting niobium coaxial cables does not significantly reduce the passive heat load[19]; as loss in the coaxial cable is not included in the below calculation, it does not lead to a significant reduction in the total heat load at the mixing chamber. Furthermore, as the coaxial cables operate in the high-frequency limit described by the telegrapher's equations, we note that the dissipated power is no longer a function of frequency. The power dissipation is given by

$$P_{COAX}(V, N) = NP_{STATIC} + \frac{0.75\left(\frac{\Delta V_{PULSE}}{4}\right)^2}{50} \quad (4)$$

Note that we have assumed that the coaxial cable drives an unterminated load with a square wave with amplitude ΔV_{PULSE} such that we can draw a direct comparison to the power dissipated with our cryo-CMOS chip.

Data availability

The datasets generated and/or analysed during the current study are available from the corresponding author upon reasonable request.

Received: 12 December 2019; Accepted: 9 December 2020;
Published online: 25 January 2021

References

1. Reiher, M., Wiebe, N., Svore, K. M., Wecker, D. & Troyer, M. Elucidating reaction mechanisms on quantum computers. *Proc. Natl Acad. Sci. USA* **114**, 7555–7560 (2017).
2. Preskill, J. Quantum computing in the NISQ era and beyond. *Quantum* **2**, 79 (2018).
3. Somma, R. D., Boixo, S., Barnum, H. & Knill, E. Quantum simulations of classical annealing processes. *Phys. Rev. Lett.* **101**, 130504 (2008).
4. Bravyi, S., Gosset, D. & König, R. Quantum advantage with shallow circuits. *Science* **362**, 308–311 (2018).
5. Aspuru-Guzik, A., Dutoi, A. D., Love, P. J. & Head-Gordon, M. Simulated quantum computation of molecular energies. *Science* **309**, 1704–1707 (2005).
6. Das, K. & Lehmann, T. Low power fast cryogenic CMOS circuit for digital readout of single electron transistor. In *Proc. Midwest Symposium on Circuits and Systems* 1–4 (IEEE, 2011).
7. Reilly, D. J. Engineering the quantum-classical interface of solid-state qubits. *npj Quantum Inf.* **1**, 15011 (2015).
8. Hornibrook, J. M. et al. Cryogenic control architecture for large-scale quantum computing. *Phys. Rev. Applied* **3**, 024010 (2015).
9. Vandersypen, L. M. K. et al. Interfacing spin qubits in quantum dots and donors—hot, dense, and coherent. *npj Quantum Inf.* **3**, 34 (2017).
10. McDermott, R. et al. Quantum–classical interface based on single flux quantum digital logic. *Quantum Sci. Technol.* **3**, 024004 (2018).
11. Bardin, J. C. et al. 29.1 A 28nm bulk-CMOS 4-to-8GHz <2mW cryogenic pulse modulator for scalable quantum computing. In *2019 IEEE International Solid-State Circuits Conference* 456–458 (IEEE, 2019).
12. Geck, L., Kruth, A., Bluhm, H., van Waasen, S. & Heinen, S. Control electronics for semiconductor spin qubits. *Quantum Sci. Technol.* **5**, 015004 (2019).
13. Patra, B. et al. Cryo-CMOS circuits and systems for quantum computing applications. *IEEE J. Solid-State Circuits* **53**, 309–321 (2018).
14. Patra, B. et al. A scalable cryo-CMOS 2-to-20GHz digitally intensive controller for 4×32 frequency multiplexed spin qubits/transmons in 22nm FinFET technology for quantum computers. In *2020 IEEE International Solid-State Circuits Conference* 304–306 (IEEE, 2020).
15. Landman, B. S. & Russo, R. L. On a pin versus block relationship for partitions of logic graphs. *IEEE Trans. Comput.* **C-20**, 1469–1479 (1971).
16. Reilly, D. J. Challenges in scaling-up the control interface of a quantum computer. In *2019 IEEE International Electron Devices Meeting* 31.7.1–31.7.6 (IEEE, 2019).
17. Wootters, W. K. & Zurek, W. H. A single quantum cannot be cloned. *Nature* **299**, 802–803 (1982).
18. Franke, D., Clarke, J., Vandersypen, L. & Veldhorst, M. Rent's rule and extensibility in quantum computing. *Microprocess. Microsy.* **67**, 1–7 (2019).
19. Krinner, S. et al. Engineering cryogenic setups for 100-qubit scale superconducting circuit systems. *EPJ Quantum Technol.* **6**, 2 (2019).
20. Arute, F. et al. Quantum supremacy using a programmable superconducting processor. *Nature* **574**, 505–510 (2019).
21. Veldhorst, M., Eenink, H. G. J., Yang, C. H. & Dzurak, A. S. Silicon CMOS architecture for a spin-based quantum computer. *Nat. Commun.* **8**, 1766 (2017).
22. Bai, Y. et al. Manufacturability and performance of 2.3-μm HgCdTe H2RG sensor chip assemblies for Euclid. In *Proc. SPIE 10709, High Energy, Optical, and Infrared Detectors for Astronomy VIII* 1070915 (SPIE, 2018).
23. Karzig, T. et al. Scalable designs for quasiparticle-poisoning-protected topological quantum computation with Majorana zero modes. *Phys. Rev. B* **95**, 235305 (2017).
24. Petta, J. R. et al. Coherent manipulation of coupled electron spins in semiconductor quantum dots. *Science* **309**, 2180–2184 (2005).
25. Casparis, L. et al. Superconducting gatemon qubit based on a proximitized two-dimensional electron gas. *Nat. Nanotechnol.* **13**, 915–919 (2018).
26. Croot, X. et al. Device architecture for coupling spin qubits via an intermediate quantum state. *Phys. Rev. Applied* **10**, 044058 (2018).
27. Hornibrook, J. M. et al. Frequency multiplexing for readout of spin qubits. *App. Phys. Lett.* **104**, 103108 (2014).
28. Das, K. & Lehmann, T. Effect of deep cryogenic temperature on silicon-on-insulator CMOS mismatch: a circuit designer's perspective. *Cryogenics* **62**, 84–93 (2014).
29. Beckers, A. et al. Characterization and modeling of 28-nm FDSOI CMOS technology down to cryogenic temperatures. *Solid State Electron.* **159**, 106–115 (2019).
30. Yang, Y., Das, K., Moini, A. & Reilly, D. J. A cryo-CMOS voltage reference in 28-nm FDSOI. *IEEE Solid-State Circuits Lett.* **3**, 186–189 (2020).
31. Reilly, D. J., Marcus, C. M., Hanson, M. P. & Gossard, A. C. Fast single-charge sensing with a rf quantum point contact. *App. Phys. Lett.* **91**, 162101 (2007).
32. Fallahi, S., Nakamura, J. R., Gardner, G. C., Yannell, M. M. & Manfra, M. J. Impact of silicon doping on low-frequency charge noise and conductance drift in GaAs/Al_xGa_{1-x}As nanostructures. *Phys. Rev. Applied* **9**, 034008 (2018).

Acknowledgements

This research was supported by Microsoft Corporation and the Australian Research Council Centre of Excellence for Engineered Quantum Systems (EQUS, CE170100009). We thank R. Rouse for help with the chip tape out and M. Cassidy, S. Waddy, C. Marcus and L. Kouwenhoven for discussions. We acknowledge the facilities as well as the scientific and technical assistance of the Research and Prototype Foundry, a Core Research Facility at the University of Sydney, and a part of the Australian National Fabrication Facility (ANFF).

Author contributions

S.J.P., K.D., A.M. and D.J.R. conceived the presented idea. K.D., A.M., Y.Y. and C.C. designed the CMOS chip and packaging. K.D., A.M., M.T., A.B. and N.D. performed the characterization experiments on the CMOS chip. The GaAs heterostructure was grown by G.C.G. and M.J.M., and the QD device was fabricated by S.J.P. S.J.P., K.D. and R.K. performed the experiment interfacing the CMOS chip to the GaAs QD device. S.J.P., K.D. and D.J.R. wrote the manuscript with input from all the authors.

Competing interests

The authors declare no competing interests.

Additional information

Extended data is available for this paper at https://doi.org/10.1038/s41928-020-00528-y.

Supplementary information The online version contains supplementary material available at https://doi.org/10.1038/s41928-020-00528-y.

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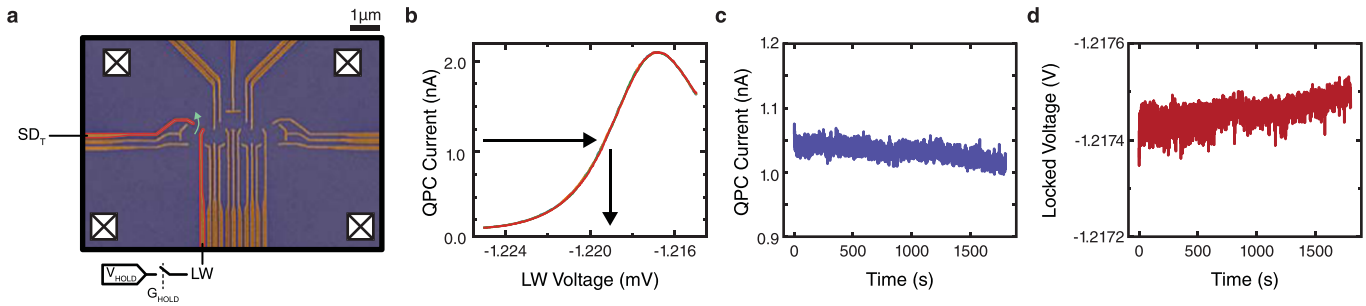
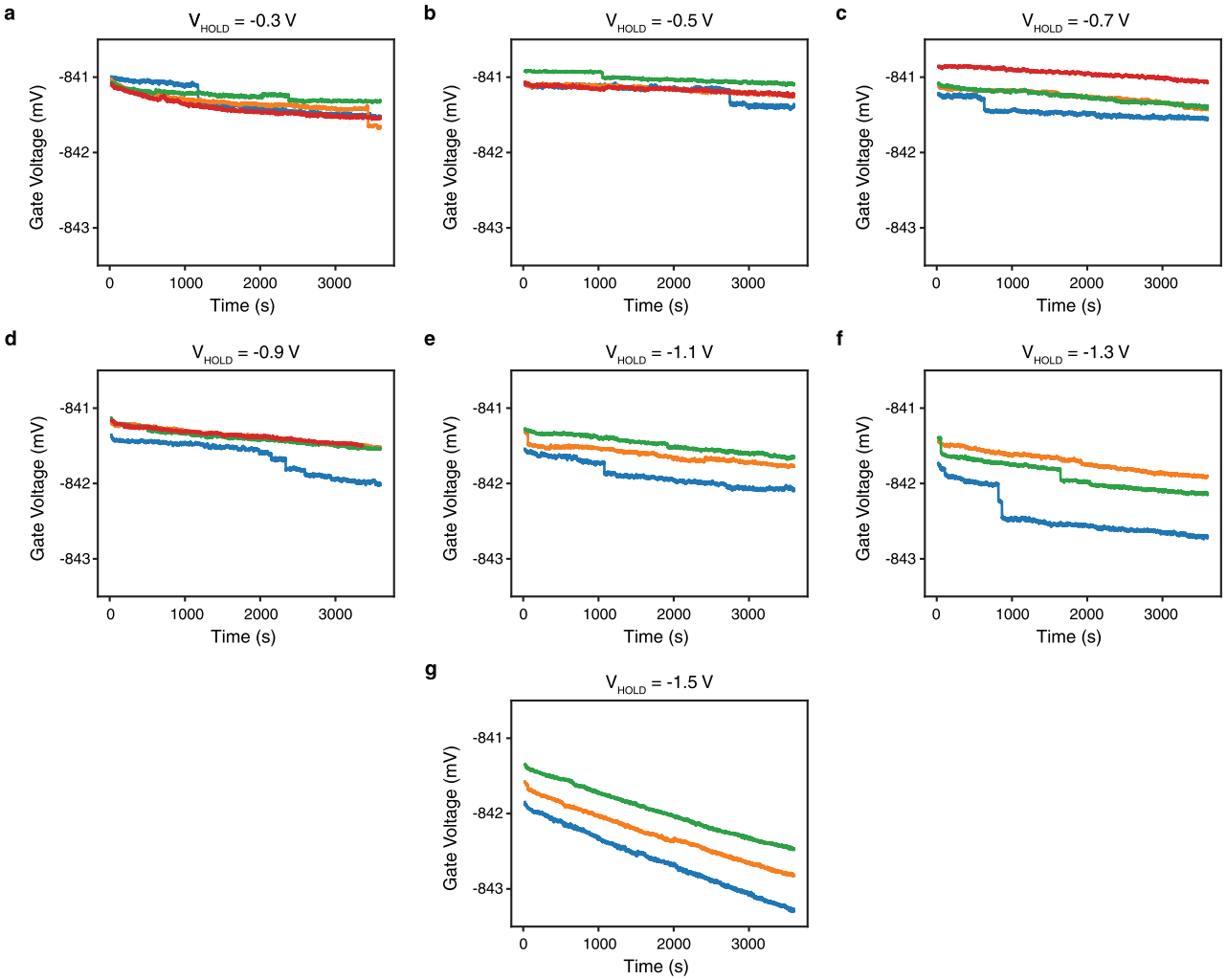
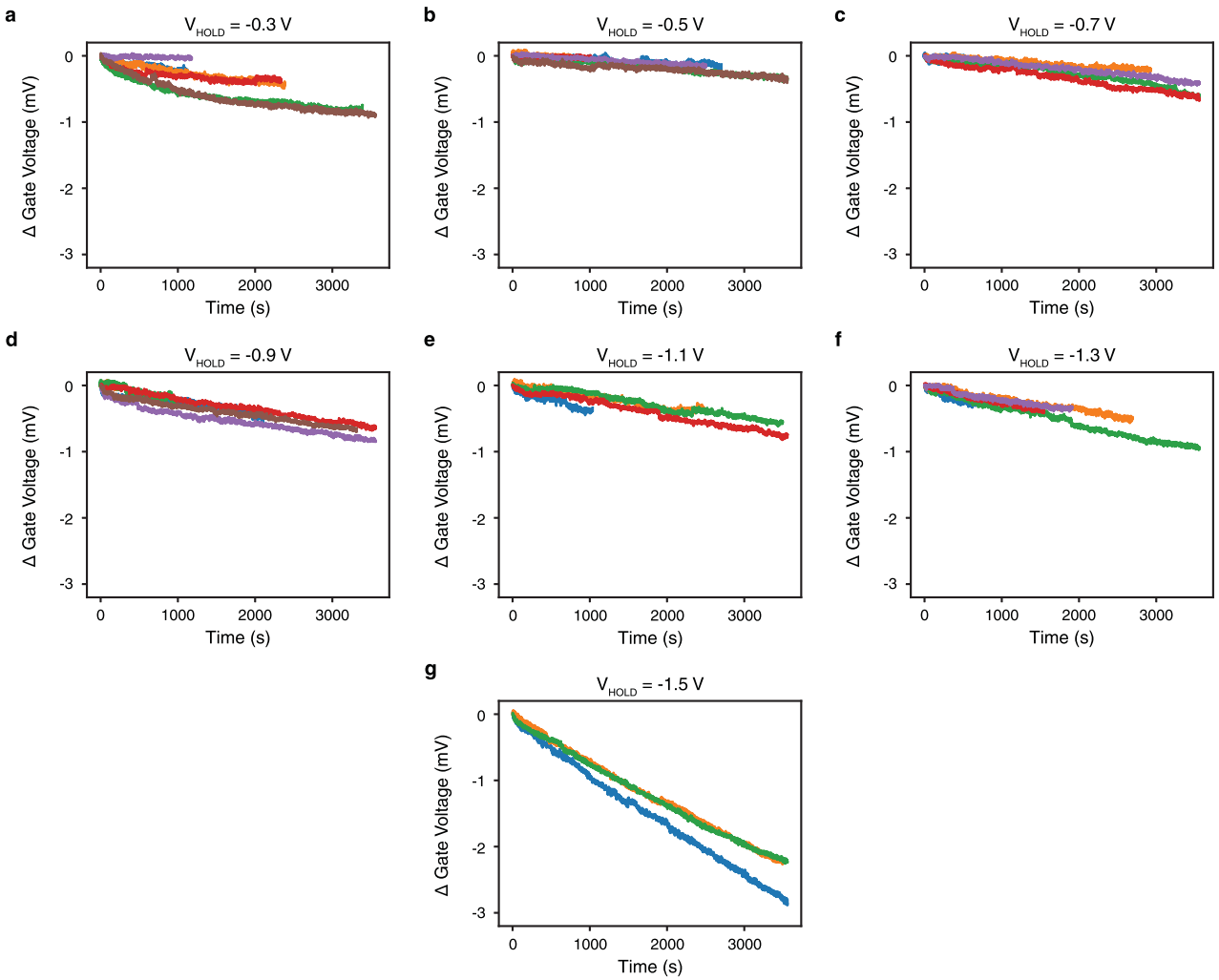


Extended Data Fig. 1 | Calibration procedure for gate leakage measurements. a, Quantum dot device used to extract gate leakage. Gates used are highlighted in red, and the current path used for the measurement is shown by the green arrow. **b**, Sample calibration trace, taken by sweeping the voltage on the LW gate, while the charge lock switch G_{HOLD} is closed. The extraction process for gate voltage is indicated by arrows. **c**, The measured current through the QPC when the charge locking switch is opened. **d**, The extracted gate voltage held on the gate for a period of 30 minutes.



Extended Data Fig. 2 | Extracted charge leakage as V_{HOLD} is varied, prior to removal of charge noise. a-g, Traces from which charge leakage is extracted in Fig. 3c, as V_{HOLD} is varied, and prior to removal of charge noise. The large steps in the extracted gate voltage are caused by low frequency charge noise in the donor layer.



Extended Data Fig. 3 | Extracted charge leakage as V_{HOLD} is varied, after removal of charge noise. a-g, Traces from which charge leakage is extracted in Fig. 3c as V_{HOLD} is varied, following the removal of charge noise. Each trace is fit with a line, from which the leakage rate is extracted.