

# Gate-Tunable Transmon Using Selective-Area-Grown Superconductor-Semiconductor Hybrid Structures on Silicon

Albert Hertel<sup>1,\*</sup>, Michaela Eichinger<sup>1,†</sup>, Laurits O. Andersen<sup>1</sup>, David M.T. van Zanten,<sup>1</sup> Sangeeth Kallatt,<sup>1</sup> Pasquale Scarlino,<sup>2</sup> Anders Kringhøj<sup>1</sup>, José M. Chavez-Garcia,<sup>1</sup> Geoffrey C. Gardner,<sup>3,4</sup> Sergei Gronin,<sup>3,4</sup> Michael J. Manfra,<sup>3,4,5,6</sup> András Gyenis,<sup>1,¶</sup> Morten Kjaergaard,<sup>1</sup> Charles M. Marcus,<sup>1</sup> and Karl D. Petersson<sup>1,2,†</sup>

<sup>1</sup>Center for Quantum Devices, Niels Bohr Institute, University of Copenhagen, 2100 Copenhagen, Denmark

<sup>2</sup>Microsoft Quantum Lab–Copenhagen, 2100 Copenhagen, Denmark

<sup>3</sup>Birck Nanotechnology Center, Purdue University, West Lafayette, Indiana 47907, USA

<sup>4</sup>Microsoft Quantum Lab–West Lafayette, West Lafayette, Indiana 47907, USA

<sup>5</sup>Department of Physics and Astronomy, Purdue University, West Lafayette, Indiana 47907, USA

<sup>6</sup>School of Materials Engineering, and School of Electrical and Computer Engineering, Purdue University, West Lafayette, Indiana 47907, USA

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We present a gate-voltage-tunable transmon qubit (gatemon) based on planar InAs nanowires that are selectively grown on a high-resistivity silicon substrate using III-V buffer layers. We show that low-loss superconducting resonators with an internal quality of  $2 \times 10^5$  can readily be realized using these substrates after the removal of buffer layers. We demonstrate coherent control and readout of a gatemon device with a relaxation time,  $T_1 \approx 700$  ns, and dephasing times,  $T_2^* \approx 20$  ns and  $T_{2,\text{echo}} \approx 1.3$   $\mu$ s. Further, we infer a high junction transparency of 0.4–0.9 from an analysis of the qubit anharmonicity.

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## I. INTRODUCTION

Superconducting qubit systems are one of the most promising approaches towards realizing a large-scale fault-tolerant quantum processor [1]. In recent years, a transmon variant that uses voltage-tunable superconductor-semiconductor hybrid Josephson junctions (JJs), the gatemon, has been developed [2,3] and realized in several material systems such as vapor-liquid-solid (VLS) nanowires [2], two-dimensional electron gases (2DEGs) [4], and graphene [5]. These junctions have an inherent nonsinusoidal current-phase relationship and can be used to create building blocks for quantum computing or as a tool for condensed matter experiments based on circuit quantum electrodynamics techniques [5–8]. Further, these

qubits can be interfaced with low dissipation cryogenic CMOS control systems [9].

In this work we demonstrate coherent operations of a gatemon qubit fabricated using a material system with selective-area-grown (SAG) Al-InAs hybrid structures [10,11] on a Si substrate that has planar III-V buffer layers. This material system has the potential to combine the individual advantages of previously demonstrated material systems [2,4,5,12] for future gatemon devices. First, similar to 2DEG-based gatemons [4], the number of JJs are relatively easy to scale as the Al-InAs nanowires are monolithically integrated into the substrate using deterministic lithographic patterning techniques. Second, the qubit capacitor, readout, and control components can be fabricated directly on the high-resistivity silicon substrate with low dielectric loss [13], similar to VLS-nanowire gatemons [2]. Similar experiments implemented on III-V substrates report a resonator quality factor of  $6 \times 10^4$  [4] or lower [4,14–16] and qubit relaxation times up to a few microseconds [4]. The main source of losses on III-V substrates can be explained by the piezoelectric photon-phonon coupling in these materials [14,15].

In this study we demonstrate that the material system can be used to make gatemons. We introduce the device design and show that high-quality resonators can be fabricated with the material system after the removal

\*a.hertel@fz-juelich.de

†karl.petersson@microsoft.com

‡First two authors contributed equally.

§Current address: Institute for Semiconductor Nanoelectronics, Peter Grünberg Institute 9, Forschungszentrum Jülich & Jülich-Aachen Research Alliance (JARA), Forschungszentrum Jülich and RWTH Aachen University, Germany.

¶Current address: Department of Electrical, Computer & Energy Engineering, University of Colorado Boulder, CO 80309, USA.

of the buffer layers. Next we show gate-tunable qubits and study the qubit anharmonicity, concluding a high junction transparency. Finally, we demonstrate coherent oscillations and extract qubit relaxation and dephasing times of a qubit device.

## II. DEVICES

Figure 1(a) shows an optical micrograph of the gatemon device. The T-shaped qubit island is capacitively coupled to a quarter-wave coplanar waveguide cavity with resonance frequency  $f_r \approx 6.6$  GHz and has a total charging energy  $E_C/h \approx 225$  MHz extracted from finite-element simulations. All parts of the readout circuit such as the cavity, transmission line, and the qubit island are fabricated on the high-resistivity (111) Si substrate with a  $4^\circ$  miscut after etching the III-V layers. The qubit island is connected to the ground plane through a JJ that is located on a mesa with dimensions  $10 \times 20 \mu\text{m}^2$  [Fig. 1(b)]. The JJ is formed by selectively wet etching an approximately 120-nm-long segment of the Al on about a 300-nm-wide Al-InAs SAG nanowire. The Josephson energy  $E_J(V_G)$  of the junction is controlled by applying a gate voltage  $V_G$  via the Al top gate that is separated from the junction by a 15-nm-thick gate dielectric ( $\text{HfO}_2$ ). The qubit frequency is given by  $f_q \approx \sqrt{8E_J(V_G)E_C}/h$  in the transmon limit ( $E_J \gg E_C$ ) [17]. The top gate and Al wires that connect the nanowire with the ground plane and qubit island climb the mesa aided by layers of cross-linked polymethylmethacrylate (PMMA) resist. In addition, the PMMA layers decouple the qubit from the III-V material of the mesa. Figure 1(c) shows a schematic of the junction region of the heterostructure along the nanowire. A schematic cross section of the nanowire is shown in the inset of Fig. 1(d). Further details of the material stack, including electrical transport characterization, are presented in Ref. [11] and briefly summarized here. The GaP/GaAs buffer is grown using metallic organic chemical vapor epitaxy and used to bridge the lattice mismatch between Si and InAs. Selective area growth [10] is used to grow planar InAs nanowires on the GaAs surface by molecular beam epitaxy [18]. To define the nanowire regions, thin films of  $\text{AlO}_x$  and  $\text{SiO}_x$  are deposited globally on the wafer and patterned using electron-beam lithography and a combination of RIE and wet-etching techniques. Inside the mask opening the InAs nanowires are grown, where the Sb-dilute GaAs buffer and  $\text{In}_{0.8}\text{Ga}_{0.2}\text{As}$  layers are used to improve the InAs quality by promoting strain relaxation [10]. The top  $\text{In}_{0.8}\text{Ga}_{0.2}\text{As}$  layer is used to prevent surface damage of the InAs layer due to device processing. A blanket Al layer is deposited *in situ* to ensure a high-quality interface between the Al and semiconductor heterostructure [19,20].

To fabricate qubit devices, most of the epitaxial Al and dielectric growth mask are removed in a first step, followed by etching the GaAs/GaP buffer and approximately

400 nm of Si to define mesa structures. The removal of the top layers of Si is necessary for the fabrication of high-quality resonators, as will be discussed in Sec. III. A detailed summary of the device fabrication can be found in Appendix A.

## III. MICROWAVE LOSS

Figure 1(e) (left panel) shows the doping profile of a Si substrate with GaP and GaAs grown on top of it

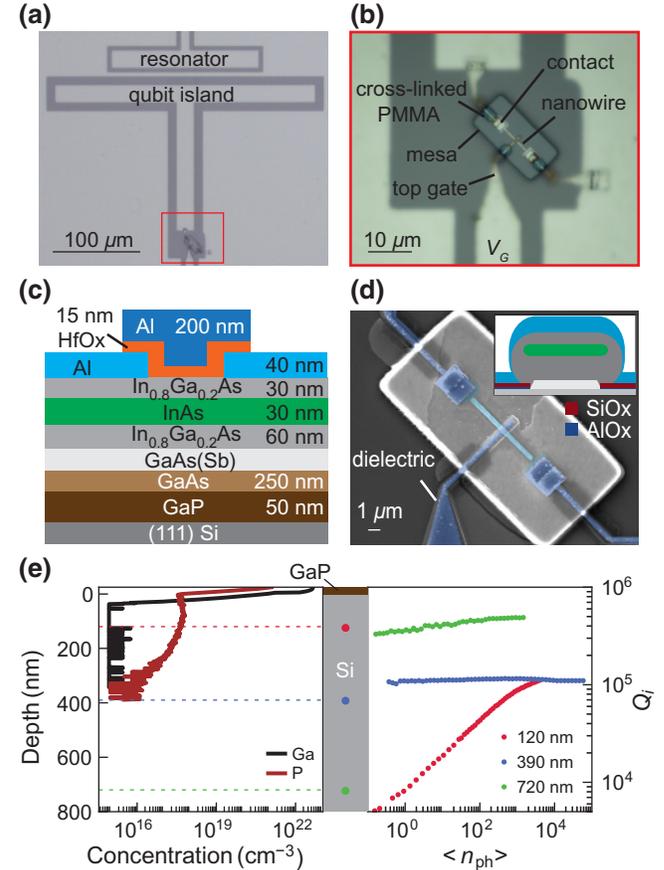


FIG. 1. Qubit devices and microwave properties. (a) Optical micrograph of the T-shaped qubit island that is capacitively coupled to a readout cavity. (b) Enlarged optical micrograph of the junction region. The junction is positioned on about a 1- $\mu\text{m}$ -thick mesa. (c) Schematic of material stack around the junction. The InAs region (green) is proximitized by the epitaxial Al (light blue) and the junction is formed by selectively removing a short segment of the Al. (d) Scanning electron micrograph of the junction area. The mesa consists of GaAs, GaP, and 400 nm of Si. The top gate metal climbs the mesa with the help of cross-linked PMMA. (inset) Cross section of the nanowire with the dielectric growth mask consisting of  $\text{SiO}_x$  and  $\text{AlO}_x$ . (e) (Left) The Ga and P concentrations of the material stack as a function of depth measured with secondary-ion mass spectrometry. (Center) Schematic of the corresponding material stack. (Right) Internal quality factor of test resonators as a function of photon number for an etch depth into the Si of 120 nm (red), 390 nm (blue), and 720 nm (green).

measured by secondary-ion mass spectrometry. The phosphorus atoms diffuse into the Si substrate during the growth process. A phosphorus concentration of  $10^{16}$ – $4 \times 10^{17}$  atoms/cm<sup>−3</sup> is measured in the top 300 nm of the Si. The gallium atoms do not diffuse far into the Si and the concentration drops below the detection limit (approximately  $10^{15}$  cm<sup>−3</sup>) within the first 20 nm. Phosphorus atoms inside the Si crystal can be considered two-level systems (TLSs) [21,22], which are one of the main limitations for the quality factor of resonators [23] and the coherence times of superconducting qubits [24].

To investigate the loss due to the phosphorus doping, we fabricate test resonators on the Si substrate after removing the III-V layers and further etching into the Si substrate (see Appendix B for further details). The extracted internal quality factor  $Q_i$  as a function of the mean photon number  $\langle n_{\text{ph}} \rangle$  for three different etch depths into the Si substrate is shown in the right panel of Fig. 1(e). For an etch depth of 120 nm, we find that  $Q_i < 10^4$  in the single-photon regime. In contrast, we find that  $Q_i \approx 1 \times 10^5$  and  $Q_i \approx 3 \times 10^5$  for etch depths 390 and 720 nm, respectively. The dielectric loss tangent associated with these quality factors can be used to define an upper bound of several microseconds for the qubit lifetime, with the exact limit depending on the qubit geometry due to the participation ratio of the electrical field at the surface and interfaces [13,24,25]. It should be noted that we measure  $Q_i \approx 2 \times 10^5$  for a designated test resonator on the qubit device chip [Figs. 1(a), 1(b), 1(d)] after the entire fabrication.

#### IV. QUBIT SPECTROSCOPY

We next demonstrate gate control of the qubit device [Figs. 1(a), 1(b), 1(d)] and study the transport across the JJ using the qubit anharmonicity; see Appendix D for measurement details. Figure 2(a) shows a two-tone spectroscopy measurement of the qubit, where we measured the resonator response  $V_H$  as a function of gate voltage  $V_G$  and drive frequency  $f_{\text{drive}}$ . Because of the relatively high on-chip drive power  $P_{\text{rf}} \approx -95$  dBm, both the  $|0\rangle \rightarrow |1\rangle$  transition at frequency  $f_{01}$  and two-photon  $|0\rangle \rightarrow |2\rangle$  transition at frequency  $f_{02}/2$  are resolved. With decreasing  $V_G$  the overall qubit frequency decreases and exhibits a nonmonotonic gate response that is typically observed for gatemon qubits [2,4–6]. We attribute the jumps in  $f_{01}$  and  $f_{02}/2$  to switches of the channel configuration in the nanowire.

The current-phase relation of a semiconductor-based JJ is nonsinusoidal and can be described with a set of channel transmission coefficients  $\{T_i\}$  consisting of a few channels with high transmission eigenvalues [26–28]. As a consequence, the gatemon anharmonicity,  $\alpha/h = 2(f_{02}/2 - f_{01})$ , in a gatemon is typically lower than for a metallic transmon [6], where  $\alpha \approx -E_C$  [17,29]. Here, we analyze  $\alpha$  following Ref. [6] to study the JJ transmission. We calculate  $\{T_i\}$  for

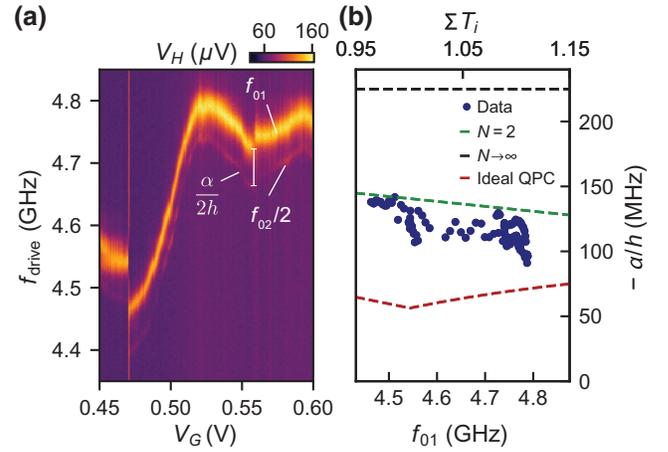


FIG. 2. Qubit anharmonicity. (a) Resonator response  $V_H$  as a function of gate top gate voltage  $V_G$  and drive frequency  $f_{\text{drive}}$ . The qubit is driven through the gate line with microwave pulses with a relatively high-power  $P_{\text{rf}}$  on chip such that the  $|0\rangle \rightarrow |1\rangle$  with frequency  $f_{01}$  and the  $|0\rangle \rightarrow |2\rangle$  with frequency  $f_{02}/2$  are measured. (b). Extracted anharmonicity  $-\alpha/h$  as a function of qubit frequency  $f_{01}$  and  $\Sigma T_i = (hf_{01})^2/(2\Delta E_C)$ . Dashed lines indicate model prediction for an ideal QPC (red), two channels with equal transmission (green), and the tunneling limit (black).

each value of gate voltage using  $\Sigma T_i = (hf_{01})^2/(2\Delta E_C)$ , where we use the measured  $\Delta = 190$   $\mu\text{eV}$  (Ref. [11]) and  $E_C/h = 225$  MHz from finite-element simulations on an intrinsic Si substrate. Assuming  $N$  transmitting channels with equal transmission probability,  $T$ , the model gives  $\alpha = -E_C[1 - 3E_J/(\Delta N)]$ . Figure 2(b) shows the anharmonicity as a function of  $f_{01}$  and  $\Sigma T_i$ . The data lie between the predicted value for  $N = 2$  channels and the ideal quantum point contact (QPC) model in which channels are filled in a steplike manner with at most one partially transmitting channel [30]. The data suggest that the transport in the observed gate range is dominated by two channels. Given equal transmission probabilities [6] this sets a lower bound  $T_{\text{min}} > \Sigma T_i/2 \sim 0.48$  on the junction transparency. Similar studies on gatemons based on VLS Al-InAs nanowires with *in situ* grown epitaxial Al (Ref. [6]), where  $-\alpha/h \approx 100$ – $150$  MHz, report two or three channels with  $T_{\text{min}} = 0.4$ – $0.9$ . This result is in good agreement with dc transport data obtained for a nominally identical material stack in Ref. [11], where we conclude a high junction transparency from measurements of the excess current and observed signatures of multiple Andreev reflections.

#### V. COHERENT OSCILLATIONS AND COHERENCE TIMES

Next, we demonstrate basic qubit control using time-domain manipulation. Figure 3(a) shows coherent Rabi oscillations with a fixed drive frequency  $f_{\text{drive}} = f_q = 4.47$  GHz where the on-chip drive power  $P_{\text{rf}}$  and the length

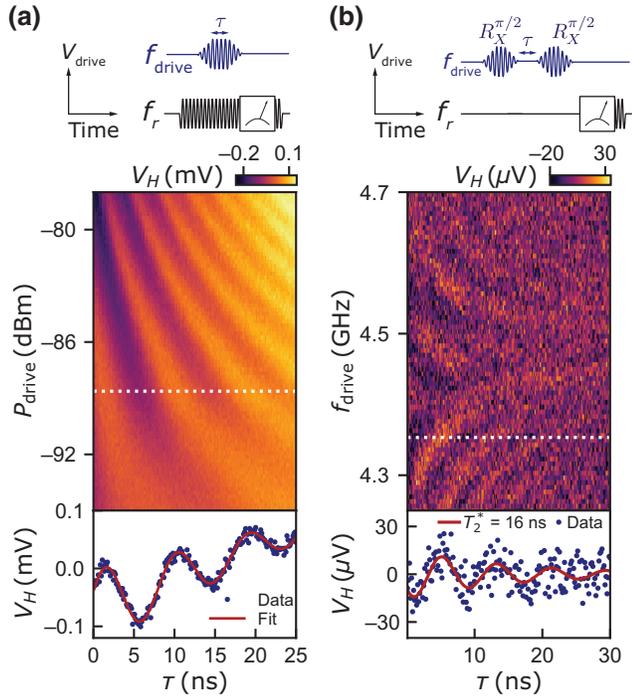


FIG. 3. Coherent oscillations. (a) The main panel shows Rabi oscillations as a function of drive power on-chip  $P_{\text{drive}}$  and pulse length  $\tau$  at fixed drive frequency  $f_{\text{drive}} = 4.47$  GHz. The pulse sequence used is shown above the plot. The lower panel shows a line cut at  $P_{\text{drive}} = -89$  dBm (white dotted line) from the main panel. The solid line is a fit to the data using a damped sinusoid with a linear contribution. (b) The main panel shows Ramsey fringes as a function of delay  $\tau$  between  $R_X^{\pi/2}$  pulses and  $f_{\text{drive}}$ . The pulse sequence is shown above. The lower panel shows a line cut at  $f_{\text{drive}} = 4.353$  GHz (white dotted line) with a fit to a damped oscillation yielding  $T_2^* \approx 15$  ns. For better visibility, we subtract the average value of  $V_H$  for each horizontal line cut in the main panels of (a) and (b).

of the qubit drive pulse  $\tau$  are varied. The lower panel of Fig. 3(a) shows the fit to the data at  $P_{\text{drive}} = -89$  dBm, where the data are described by a damped sinusoid with a linear increase. A likely explanation of this additional linear increase in  $V_H$  [Fig. 3(a)] is leakage to higher level states [31]. We discuss the Rabi oscillations further in Appendix C. Appendix D provides additional details on the pulsed measurements.

Figure 3(b) shows Ramsey fringes measured by using two  $R_X^{\pi/2}$  pulses separated by a delay  $\tau$ . The lower panel of the figure shows a fit of a damped sinusoid to a line cut of the data. From the fit we extract a dephasing time  $T_2^* \approx 15$  ns. The extracted value is in good agreement with estimates of  $T_2^*$  from a fit to the power dependence of the qubit linewidth in spectroscopy, as described in Ref. [32] (see Appendix E).

Figure 4(a) shows the pulse sequences that we use to measure the qubit lifetimes. We use overlapping drive and

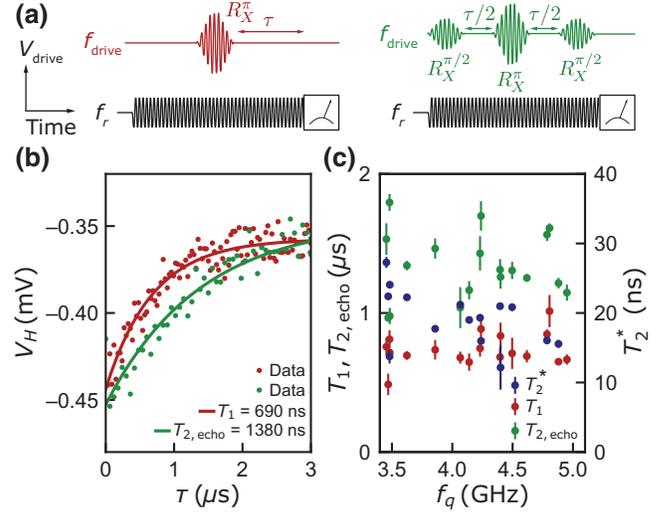


FIG. 4. Qubit lifetimes. (a) Pulse sequences for lifetime measurements. (b) The  $T_1$  and  $T_{2,\text{echo}}$  measurements of the qubit at  $f_q \approx 4.48$  GHz. The  $T_{2,\text{echo}}$  data are offset by  $+0.09$  mV. (c) Lifetimes as a function of  $f_q$ . The  $T_1$  and  $T_{2,\text{echo}}$  times are measured with the pulse sequences shown in (a). The  $T_2^*$  time is extracted from the power dependence of the linewidth of the qubit in spectroscopy (Appendix E).

readout pulses to increase the signal-to-noise ratio as the  $T_2^*$  time is shorter than the ring-up time of the readout resonator  $\tau_{\text{rise}} \approx 480$  ns (see Appendix D). Figure 4(b) shows representative measurements of  $T_1$  (red) and  $T_{2,\text{echo}}$  (green) using a Hahn echo sequence with fits to an exponential decay.

Figure 4(c) shows the measured lifetimes for qubit frequencies between 3.5 and 5.0 GHz. The  $T_1$  and  $T_{2,\text{echo}}$  times are obtained from calibrated pulses and  $T_2^*$  is estimated from the qubit linewidth (Appendix E). The extracted mean values are  $\bar{T}_1 = 740 \pm 110$  ns,  $\bar{T}_2^* = 21 \pm 7$  ns, and  $\bar{T}_{2,\text{echo}} = 1340 \pm 230$  ns. The  $\bar{T}_1$  and  $\bar{T}_{2,\text{echo}}$  times are comparable with the lifetimes extracted for gatemon fabricated with VLS nanowires on a Si substrate [2]. However, an order of magnitude longer  $T_2^* \approx 900$  ns was reported for those devices [2,12].

## VI. DISCUSSION AND CONCLUSIONS

The measured dephasing times indicate that dephasing is limited by low-frequency noise since  $T_{2,\text{echo}} \gg T_2^*$ . We suspect that both the gate dielectric and dielectric close to the junction used for the selective area growth [11] cause the low decoherence times. Comparing previous Al-InAs-based gatemon architectures, VLS-nanowire gatemons [2,12] reported longer dephasing times ( $T_{2,\text{VLS}}^* \approx 0.9\text{--}3.7$   $\mu\text{s}$ ) than gatemons based on 2DEGs [4] ( $T_{2,2\text{DEG}}^* \approx 400$  ns) that are longer than the dephasing times in this work ( $T_{2,\text{SAG}}^* \approx 20$  ns). For the VLS-nanowire gatemon, the nanowire is placed on the device chip without

additional dielectrics near the active junction region. In case of the 2DEG gatemon, mesa material below the proximitized InAs channel and gate dielectric are still present near the junction on the qubit chip after device fabrication. Further, the mesa with a width of approximately  $1\ \mu\text{m}$  is smaller than the mesa in this work (about  $10\ \mu\text{m}$ ). The main difference in this work is the presence of the residual growth dielectric with a low quality near the junction. The  $\text{SiO}_x$  layer in particular is optimized to have a low crystal quality to increase the selectivity of the InAs growth [10]. We expect this layer to have an increased TLS density compared to the mesa material and, thus, limit  $T_2^*$ .

The relaxation times of the qubits are lower than the relaxation times of the test resonator, indicating that  $T_1$  is not limited by the dielectric loss of the substrate. Based on the internal quality factor measured for readout resonators  $Q_i = 2 \times 10^5$ , we expect the upper limit for the relaxation time of a qubit with frequency  $f_q = 5\ \text{GHz}$  to be  $T_1 \approx Q_i / (2\pi f_q) \approx 6\ \mu\text{s}$ . This suggests that the qubit is possibly limited by dielectric loss due to the III-V material or doped Si in the mesa region. Although we do not expect that the doping level is high enough for the doped Si to be conducting, we cannot exclude the possibility that normal conducting channels exist near the GaP/Si interface.

To improve  $T_2^*$ , the material quality near the junction needs to be improved. Further, the qubit can be better decoupled from the mesa by means of device design which leads to a reduced participation ratio [13,25,33] and, therefore, increased relaxation times. Potential changes in device fabrication and design are summarized in Appendix G. Other potential sources of decoherence such as gate noise and readout are discussed in Appendix H.

In summary, we have demonstrated that selective-area-grown Al-InAs nanowires on a Si substrate are a platform for voltage-controlled transmon qubits. We implemented the SAG-based gatemon on a low-loss substrate with relaxation times of roughly  $700\ \text{ns}$  and dephasing times of  $20\ \text{ns}$ . With a further improvement of coherence, this material platform opens possibilities for scalable highly integrated quantum circuits such as gatemons [2], protected qubits [8], voltage-tunable quantum buses [34], and voltage-tunable quantum memories [35].

## ACKNOWLEDGMENTS

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## APPENDIX A: QUBIT DEVICE FABRICATION

The qubit devices are fabricated using a combination of standard electron-beam lithography and UV lithography. At the beginning of the qubit fabrication, the entire

chip is covered with a  $40\text{-nm}$ -thick Al film on top of the dielectric layers consisting of  $10\text{-nm}$ -thick  $\text{SiO}_x$  and  $5\text{-nm}$ -thick  $\text{AlO}_x$ . In a first step, Al is etched selectively on the device chips using Al etchant Transene D, only leaving Al in dumbbell-shaped areas around nanowires [Fig. 1(b)]. Using the same resist stack, both  $\text{SiO}_x$  and  $\text{AlO}_x$  are etched using a buffered HF solution. The dumbbell shape offers a compromise between little dielectric and Al being left around the nanowire [see Fig. 1(b)] and sufficiently large MBE Al patches with an area of approximately  $1\ \mu\text{m}^2$  that are used to connect the Al-InAs nanowires to the rest of the circuit. Next, the mesa is defined by protecting the nanowire and a small surrounding area with photoresist (AZ5214E) while removing GaAs, GaP, and approximately  $400\ \text{nm}$  of Si using two reactive ion etching steps. First, an etch with process gases  $\text{Cl}_2$  and Ar is used to create an almost vertical mesa profile. The second etch, which uses process gases  $\text{Cl}_2$  and  $\text{N}_2$ , creates a trapezoidal mesa profile [see Fig. 1(d)]. The first step is optimized to etch the material stack fast, reducing heat load of the resist during the process, and creating steep side walls. The second step creates a trapezoidal shape, which is beneficial for the crawl up of the top gate metal. Then, the JJ is defined by selectively removing an approximately  $150\text{-nm}$ -long Al segment on the nanowire using Transene Al etchant type D at  $50^\circ\text{C}$ . Next, Al is evaporated with a lift-off process, where the mesas are still protected by resist. The evaporation is preceded by a  $10\ \text{s}$  long dip in a buffered HF solution to remove surface oxides from the chip. The transmission line, readout resonators, qubit islands, a test resonator, and gate lines are defined by selectively removing Al with a wet-etch solution (Transene Al etchant type D at  $50^\circ\text{C}$ ). Next,  $15\text{-nm}$   $\text{HfO}_2$  is grown by atomic layer deposition in lithographically predefined regions on top of the JJs. Additionally,  $\text{HfO}_2$  is deposited in areas where Al will climb mesas to ensure they are isolated. In these climbing areas PMMA bridges are defined by crosslinking PMMA through the exposure with 30 times the area dose that is typically used to pattern the resist [see Fig. 1(d)]. Next, gates ( $200\text{-nm}$ -thick Al) are evaporated. These are later used to tune the critical currents of the single JJs and thereby the qubit frequencies. In addition, Al wires leading from the nanowire to qubit islands and nanowire to the ground plane are deposited. In the final step, the nanowire, qubit island, and ground plane are electrically connected by creating ohmic contacts. To ensure a good contact,  $\text{AlO}_x$  on the Al wires and MBE Al is removed by Ar-milling prior to the deposition of an approximately  $250\text{-nm}$ -thick Al layer.

## APPENDIX B: RESONATOR FABRICATION AND MEASUREMENTS

The Al test resonators are fabricated on the Si substrate after removing the entire GaAs and GaP buffer and deep

TABLE I. Three resonator devices fabricated on Si with different etching parameters and their extracted resonance frequency  $f_r$ , external quality factor  $Q_{\text{ext}}$ , and internal quality factor  $Q_i$ .

Sample	Etch depth (nm)	$f_r$ (GHz)	$Q_{\text{ext}}$ ( $10^3$ )	$Q_i$ ( $10^3$ )
1	120	6.35	12	27
2	390	5.46	20	102
3	720	5.51	57	371

etching into the Si substrate using the RIE steps described above. We also add patterned structures on the chip to measure the etch depth with a mechanical profilometer. The resonators are then defined by a global electron-beam evaporation of 100-nm-thick Al under high vacuum and subsequent selective etching of the Al using standard electron  $e$ -beam lithography and wet-etch techniques. Preceding the Al deposition, the device chip is dipped into a buffered HF solution to remove surface oxides from the Si substrate.

For the extraction of the internal and external quality factors,  $Q_i$  and  $Q_{\text{ext}}$ , we use the fit procedure described in Ref. [36]. Figure 5 shows an example fit in the few-photon regime for a resonator made after etching the III-V layers and 720 nm of Si. Here, we use resonators for which  $Q_{\text{ext}} \approx Q_i$  in the few-photon regime. The data shown in Fig. 5 are taken at  $P_{\text{on chip}} = -149$  dBm, which corresponds to a mean photon number on chip of  $\langle n_{\text{ph}} \rangle \approx 1$ . The resonance frequency  $f_r$  of the resonator is at  $f_r = 5.51$  GHz. From the fit we extract  $Q_i \approx 3.6 \times 10^5$  and  $Q_{\text{ext}} \approx 57 \times 10^3$ . We note that, for extracting  $Q_i$ , we use resonators for which the external quality factor  $Q_{\text{ext}}$  matches  $Q_i$  ( $Q_{\text{ext}} \approx Q_i$ ) in the few-photon regime.

We measure three resonator devices with different etch times. The results are summarized in Table I. The quality factor for device 1 is extracted from a fit at  $P_{\text{on chip}} = -125$  dBm, for device 2 at  $P_{\text{on chip}} = -146$  dBm, and for device 3 at  $P_{\text{on chip}} = -148$  dBm.

### APPENDIX C: RABI OSCILLATIONS

Figure 6(a) shows a typical chevron pattern measured at the same operating point in gate voltage as the data shown in Fig. 3(a). In Fig. 6(b) we replot the data from Fig. 3(a) with the vertical axis rescaled in terms of drive amplitude,  $V_{\text{drive}}$ . The extracted Rabi frequency  $\Omega_{\text{Rabi}}$  against drive amplitude is shown in Fig. 3(c). For a qubit system, one expects  $\Omega_{\text{Rabi}} \propto V_{\text{drive}}$ ; however, as indicated, the data can only be described by a linear fit for low powers  $V_{\text{drive}} < 8 \mu\text{V}$ . We attribute this observation—as well as the linear increase in the signal as a function of  $\tau$ —to leakage to higher order states. Even at the lowest drive power  $f_{\text{Rabi}} \approx -\alpha/h$ , and for increasing power and faster  $\Omega_{\text{Rabi}}$  we

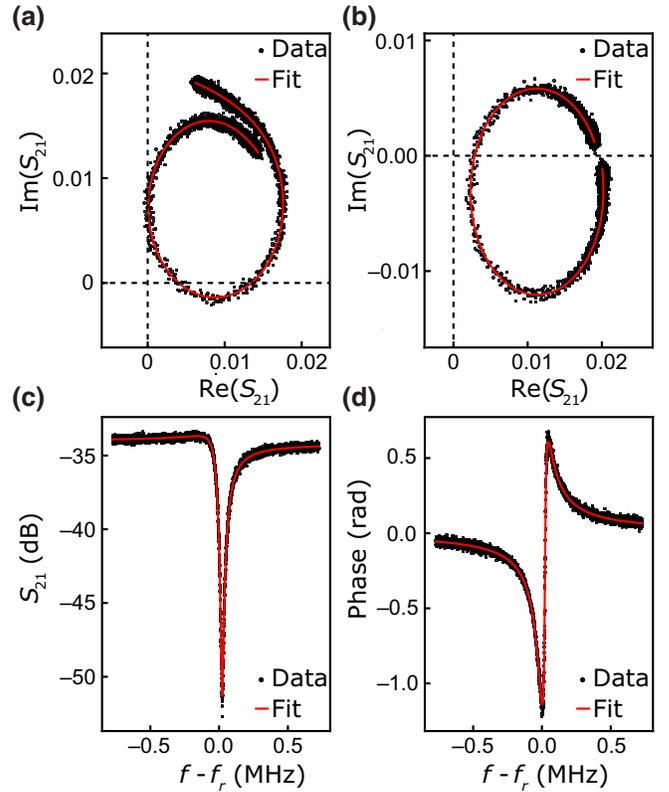


FIG. 5. Example data and fit of the resonator with an etch depth of 720 nm (see Fig. 1) at  $P_{\text{on chip}} = -149$  dBm. (a) Raw data (black) and fit (red) of the trajectory of  $S_{21}$  in the complex plane. (b) The  $S_{21}$  data and fit after correcting for the cable delay [36,37]. Panels (c) and (d) show the magnitude and phase of  $S_{21}$  of the data in (a) with the corresponding fits.

observe an increased deviation from the expected dependence  $\Omega_{\text{Rabi}} \propto V_{\text{drive}}$  and increasing signal background. A similar result is reported in Ref. [38].

We numerically simulate the behavior of a strongly driven four-level system in a rotating-wave approximation using the QuTip package [39]. The anharmonicity of the four-level system is 225 MHz, the external drive is on resonance with the 0–1 transition and turns on with a square edge, the  $T_1$  decay constant between the 0–1 states is 600 ns, between the 1–2 states is 300 ns, and between the 2–3 states is 200 ns. In Fig. 6(d) we plot the Rabi frequency, which is extracted from the time scale when the population of the ground state is minimal, as a function of drive amplitude. While in a two-level system the Rabi frequency scales linearly with the drive amplitude, in a multilevel system the Rabi rate deviates from this behavior due to leakage to higher states, as shown by our simulation. We truncate the simulations at a drive frequency  $\Omega_{\text{drive}}/2\pi = 200$  MHz as accurate simulations need a more sophisticated model with more energy levels and without the use of the rotating-wave approximation.

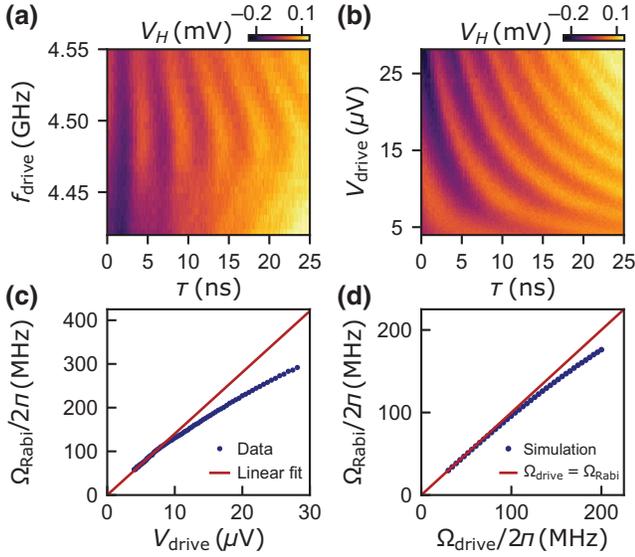


FIG. 6. Coherent oscillations. (a) Rabi oscillations as a function of  $f_{\text{drive}}$  at the same gate point as in Fig. 3(a) and  $P_{\text{drive}} = -82$  dBm. (b) Rabi oscillations from Fig. 3(a) with the on-chip drive amplitude  $V_{\text{drive}}$ . (c) Extracted Rabi frequency  $\Omega_{\text{Rabi}}/2\pi$  as a function of  $V_{\text{drive}}$ . The red line is a linear fit of the form  $\Omega_{\text{Rabi}}/2\pi = m \cdot V_{\text{drive}}$  for  $V_{\text{drive}} < 8.1 \mu\text{V}$ , with  $m$  the fit parameter. (d) Simulated Rabi frequency  $\Omega_{\text{Rabi}}/2\pi$  of a four-level system (blue dots) compared with the Rabi frequency of a two-level system (red line).

#### APPENDIX D: PULSED QUBIT MEASUREMENTS

All measurements in this work are performed with the qubit in the transmon limit ( $E_J \gg E_C$ ) and in the dispersive regime  $|f_q - f_r| \gg g/2\pi$ , where  $g/2\pi \approx 80$  MHz is the coupling between the cavity and qubit island. In all experiments, the dc gate voltage  $V_G$  and the rf drive tone for the qubit are combined using a bias tee at the millikelvin stage of the dilution refrigerator and applied through the gate line.

We extract the frequencies  $f_{02}/2$  and  $f_{01}$  [Fig. 2(a)] by numerically fitting two independent Lorentzian line shapes to the signal and using the position of peak maxima as transition frequencies. For all qubit measurements in this work, the pulse length  $\tau$  corresponds to the length of the plateau of a Gaussian flat top pulse with a rise time of  $2\sigma = 4$  ns. All measurements in this work are limited to pulse lengths of approximately 30 ns due to the short dephasing time (see Sec. V). To increase signal-to-noise ratio and adjust for short qubit dephasing times as well as a low coupling between resonator and transmission line ( $Q_c \approx 2 \times 10^4$ ), the resonator is driven during the qubit manipulation and resonator readout [pulse sequence shown in Fig. 3(a)] unless stated otherwise. Here, we estimate that the signal rise time of the resonator with  $f_{\text{res}} \approx 6$  GHz is  $\tau_{\text{rise}} \approx Q_c/2\pi f_{\text{res}} \sim 480$  ns. A nonoverlapping pulse sequence in

which the resonator drive is applied when the signal integration is started is used to measure the data in Fig. 3(b) (Ramsey fringes). Measurements as shown in Fig. 3(a) are used to calibrate  $R_X^\pi$  and  $R_X^{\pi/2}$  pulses that rotate the qubit state around the  $x$  axis by  $\pi$  and  $\pi/2$ .

We note that, for our qubit, the  $T_2^*$  time (approximately 15 ns) is shorter than the ring-up time of the readout resonator (approximately 480 ns) and comparable to the minimum gate time to avoid state leakage, about  $1/(|\alpha|/h)$ . In a standard gate time measurement including a  $\pi$  pulse [see Figs. 7(c) and 7(d)] this can lead to leakage to higher order states. When driving we observe an additional slow oscillation in  $V_H$  (not shown) that we attribute to driving chip modes that are coupled to the qubit. The observed linear increase can be the onset of this slow oscillation. To test if the relaxation times are limited by leakage to higher order states, we perform additional weak spectroscopy measurements. For these, we use a weak spectroscopy pulse as drive tone, as shown in Figs. 7(a) and 7(b). Here, a low readout power is used to avoid an ac-Stark shift of the qubit caused by a high photon population in the resonator. Figure 7(e) compares the relaxation times extracted from the different datasets and their respective exponential fit as illustrated in Figs. 7(a)–7(d). The pulsed measurement results [Figs. 7(c) and 7(d)] are in good agreement with the weak drive measurements.

#### APPENDIX E: CONTINUOUS DRIVE $T_2^*$ MEASUREMENT

To estimate the dephasing time of the qubit, we follow the method described in Ref. [32]. Here, the linewidth of the qubit in spectroscopy can be described by the equation  $2\pi \delta_{\text{HWHM}} = 1/T_2' = (1/T_2^{*2} + n_s w_{\text{vac}}^2 T_1/T_2^*)^{1/2}$ , where  $\delta_{\text{HWHM}}$  is the half width at half maximum of the spectroscopy feature,  $T_2'$  is the dephasing time, and  $n_s w_{\text{vac}}^2$  is proportional to the drive power on-chip  $P_{\text{drive},s}$  with  $P_{\text{drive},s} = P_{\text{drive}} - 60$  dB (60 dB accounts for cryogenic attenuators, line attenuation, and filtering as depicted in Fig. 10), and  $T_2^*$  is the dephasing time at zero drive power. Figure 8(a) shows the spectroscopy signal as a function of  $P_{\text{drive},s}$ . At each value of  $P_{\text{drive},s}$  we extract the linewidth by fitting to a Lorentzian line shape [Fig. 8(b)]. As shown in Fig. 8(c),  $T_2^*$  is extracted from a fit to the power dependence of the linewidth.

#### APPENDIX F: GATE-VOLTAGE DEPENDENCE

We perform  $T_1$  measurements and spectroscopy sweeps to extract  $T_2^*$  from the linewidth at different gate voltages. In Fig. 9(a) we show the spectroscopy signal for gate voltages  $-0.09 \text{ V} < V_G < 0.3 \text{ V}$ . In this range  $3.6 \text{ GHz} < f_q(V_G) < 4.8 \text{ GHz}$ . In Figs. 9(b) and 9(c) the relaxation time  $T_1$  and dephasing time  $T_2^*$  are shown for 20 different values of  $V_G$  and the qubit frequency  $f_q(V_G)$  which

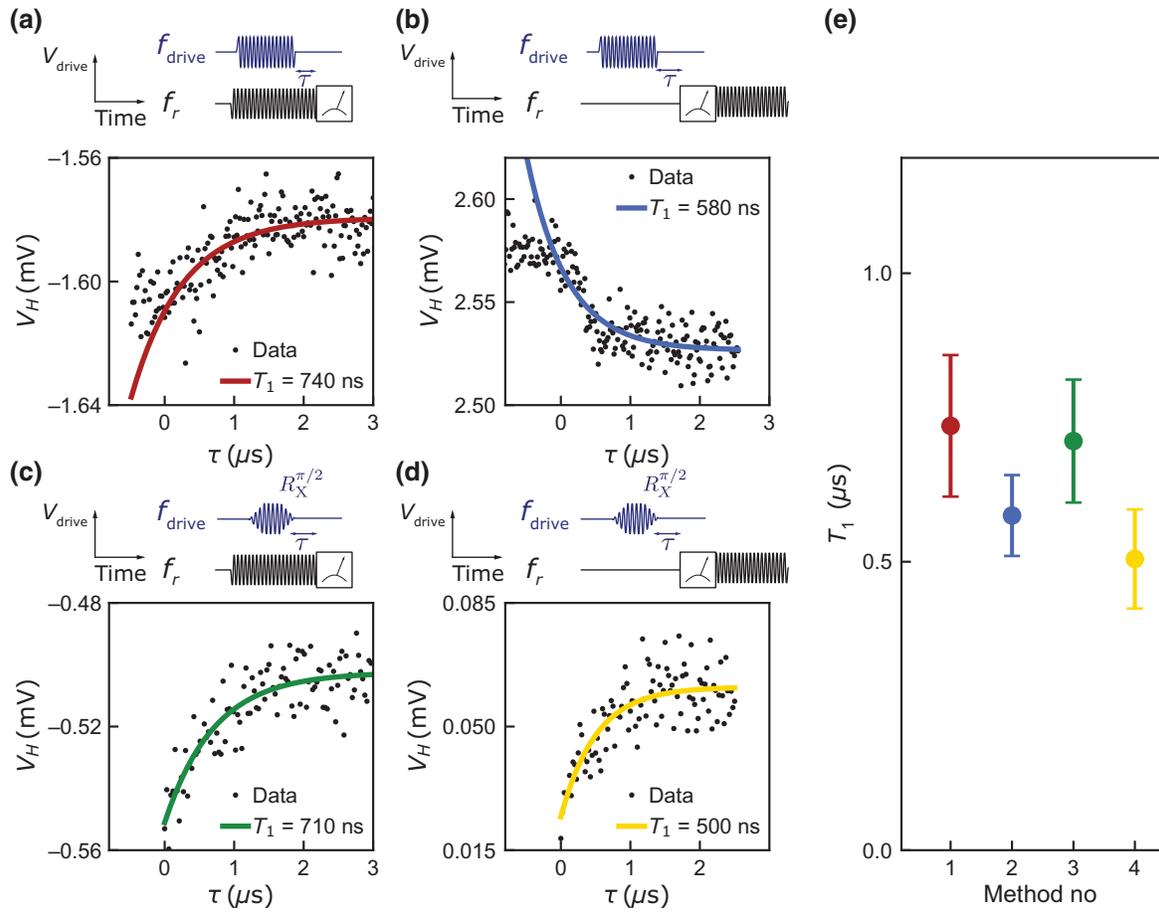


FIG. 7. Different measurement methods for extraction of relaxation time  $T_1$ . (a) Readout and weak spectroscopy drive tone overlap. (b) The strong readout tone is applied after the spectroscopy drive tone. (c) A  $\pi$  pulse is used to excite the qubit. This drive tone overlaps with the readout tone. (d) The readout tone is applied after the  $\pi$  pulse. (e) Comparison of extracted  $T_1$  values from datasets (a)–(d).

we extract from the spectroscopy data. Figure 9(d) shows  $T_1$  and  $T_2^*$  as a function of gate dispersion  $df_q/dV_G$  calculated numerically from  $f_q(V_G)$ . As  $T_1$  and  $T_2^*$  show no

correlation with qubit frequency  $f_q(V_G)$ , we conclude that the qubit coherence times are not limited by gate noise. The independence of  $T_2^*$  from gate dispersion is also reported

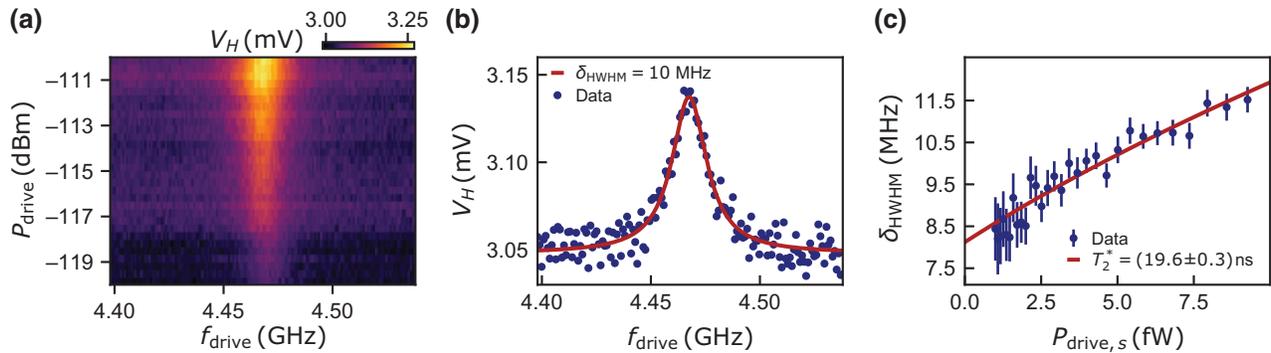


FIG. 8. Spectroscopy data for estimation of dephasing time  $T_2^*$ . (a) Spectroscopy signal as a function of qubit drive  $P_{\text{drive},s}$  and drive frequency  $f_{\text{drive}}$ . (b) Line cut from (a) at  $P_{\text{drive},s} = -116.7$  dBm with fit to a Lorentzian line shape (purple line). (c) Qubit linewidth  $\delta_{\text{HWHM}}$  versus power  $P_{\text{drive},s}$  with fit using  $2\pi \delta_{\text{HWHM}} = 1/T_2^* = (1/T_2^{*2} + n_s w_{\text{vac}}^2 T_1/T_2^*)^{1/2}$ . The decoherence time is estimated from the intersection of the fit with the y axis.

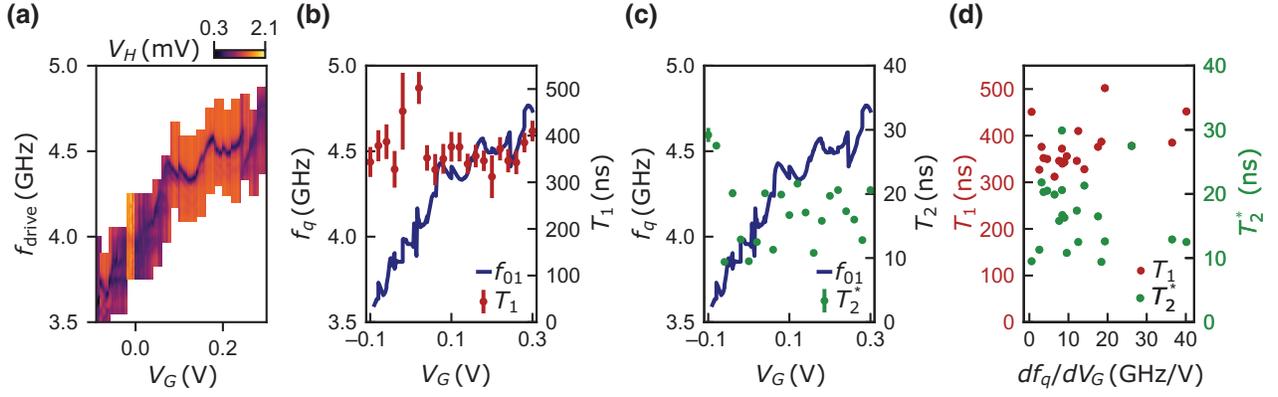


FIG. 9. Coherence times and  $f_q$  as a function of  $V_G$ . (a) Spectroscopy signal. (b) The qubit frequency  $f_q$  as a function of  $V_G$  and  $T_1$  for 20 different gate voltages. (c) Same as (b) but for  $T_2^*$ . (d) Coherence times  $T_1$  and  $T_2^*$  as a function of gate dispersion  $df_q/dV_G$ .

in Ref. [12] for VLS-nanowire gatemons with  $T_2^*$  up to  $4 \mu\text{s}$ .

### APPENDIX G: POTENTIAL FABRICATION IMPROVEMENTS

The mesa can be placed further away from strong electric fields generated by the qubit island and the mesa size can be reduced. This can be achieved by using a different dry etch chemistry. An isotropic wet etch can be used to create a concave mesa shape, leading to an increased distance and, thus, smaller coupling between the mesa and the residual circuit. A possible improvement for future devices is the definition of the mesa before the selective area growth, leading to a reduced mesa size, set by the diffusion length of particles during the MBE growth, and enabling the fabrication of the readout circuit and qubit island using MBE Al. Side gates can be used instead of top gates to remove gate dielectric from the process flow. The growth dielectric around nanowires can be removed by means of HF vapor etching or design changes. In order to decouple qubits from the lossy mesa stack, thicker PMMA bridges can be used.

### APPENDIX H: ADDITIONAL SOURCES FOR DECOHERENCE

We can exclude setup-related and measurement-related dephasing mechanisms as limiting factors for the short dephasing times. Our system is calibrated with metallic fixed-frequency transmon devices, where  $T_2^* \approx 10 \mu\text{s}$  is measured, and we use the same sample packaging as in Refs. [2,4], where  $T_2^* \approx 900 \text{ ns}$  and  $T_2^* \approx 400 \text{ ns}$  are reported. Further, no correlation between the  $T_2^*$  and the gate dispersion  $df_q/dV_G$  is observed, indicating lifetimes are not limited by decay through the gate line or gate noise (Appendix F). We did not observe a correlation between  $T_2^*$  and the gate dispersion in a previous work

on VLS-nanowire gatemons either [12], with the differences that the  $T_2^*$  were of the order of several microseconds and no dielectric layers near the active junction region were used. We assume that the short  $T_2^*$  in this work can be explained by dephasing due to TLS inside and at the surface of the growth dielectric near the nanowire. The recovery  $T_{2,\text{echo}} \approx 2T_1$  with a single echo pulse suggests a slow  $1/f$ -type noise spectrum which is consistent with the TLS interpretation [40].

We note that the Rabi frequencies in these measurements are comparable to the qubit anharmonicity  $|\alpha|/h \sim 120 \text{ MHz}$ , potentially leading to leakage to higher order states and inducing dephasing [31]. To reduce the potential impact of this effect, Gaussian flat-top pulses are used to avoid driving higher order transition of the qubit system. To avoid additional dephasing due to photon number fluctuations, we chose a low cavity readout power. Further, we confirm that this overlapping pulse sequence yields the same lifetimes as alternative measurement techniques where we use nonoverlapping pulses or prepare the qubit in a well-defined mixed state using long and weak spectroscopy pulses [38] (see Appendix D).

### APPENDIX I: SETUP

The presented measurements are acquired in a cryofree dilution refrigerator with a base temperature of about  $30 \text{ mK}$ . Figure 10 shows a detailed schematic of the experimental setup. An rf switch is used to route signals to the sample that are either coming from the vector network analyzer (VNA) or from AWG modulated rf sources. The input signals are attenuated and filtered before reaching the sample. For measurements, the rf switch can direct the readout signal back to the VNA or to the demodulation circuit. The latter consists of a mixer for down-conversion of the output signal to an intermediate frequency by mixing it with a reference tone. The signal is then filtered and amplified before it is finally digitized and digitally

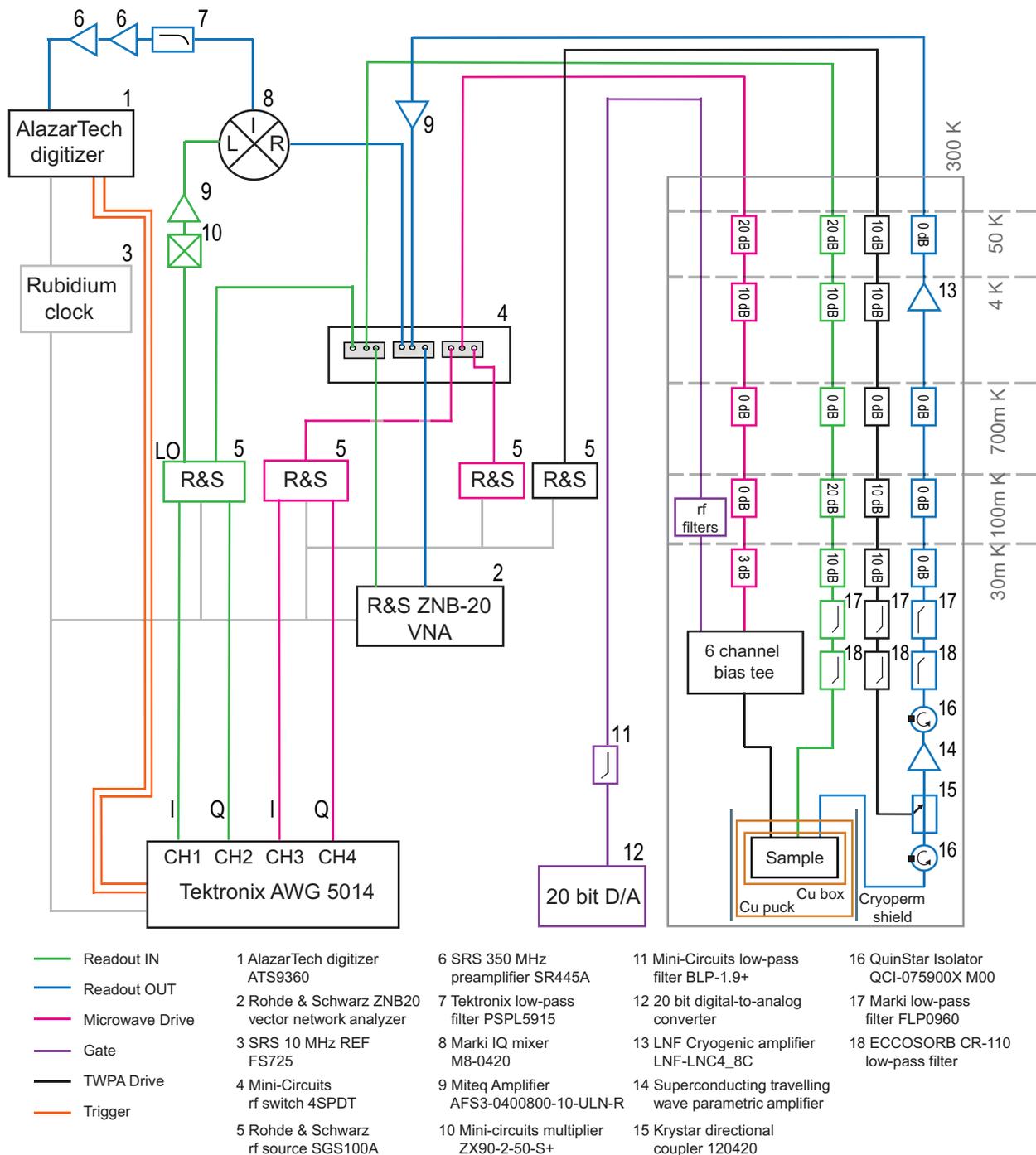


FIG. 10. Schematic of the experimental setup used for the experiments. The readout resonator can be driven by a vector network analyzer (VNA) or by a signal from a rf source that is modulated by an arbitrary waveform generator (AWG) (blue line). The amplified output signal can be read out either by the VNA or undergo down-conversion by mixing with a reference signal. Microwave equipment is synchronized using a 10-MHz clock reference. To tune the chemical potential of the SAG nanowire junction, a dc line (purple) is connected to the sample. The dc signal merges with the (pink) rf signal used for driving the qubit in a bias tee channel.

downconverted with the AlazarTech digitizer. The microwave drive tone is generated by an additional R&S microwave source and is applied via its own drive line

that merges with the gate line in a bias tee before reaching the sample. For synchronization of all instruments, an SR FS725 10 MHz clock reference is used.

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